On-Chip Power Stage and Gate Driver for Fast Switching Applications

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***Abstract*— The demand for low-cost integrated circuits for automotive applications is increasing, while their cost must remain low to keep the product competitive. In this scenario, a high-speed monolithic integrated circuit to control a load current is here proposed. It is composed by a level shifter and a gate driver for a high power switch in a DC-DC Buck converter to be realized in a low cost technology. For chip area reduction, an n-channel vertical power transistor is chosen as power transistor. High switching frequency (up to 1MHz) can be used to reduce external components size. The device is optimized to achieve 94.4% efficiency. Implementation concept, schematic and layout will be shown.**

***Keywords*— gate driver, DC/DC converter, Buck,**

I. Introduction

Day-by-day the demand for switching DC-DC converters is increasing over conventional converters because of their higher efficiency. The continuous growing markets in electric vehicles, renewable energy system and high-brightness LED lighting systems, etc, create a big demand for new systems that can operate with High-Voltage (HV) and higher power levels. To maintain the cost of such systems competitive, integrated circuits are requested, integrating as much as possible external components, or operating with external components of reduced size. In case of switching converters, this involves increasing the switching frequency of the power MOSFET up 1MHz, keeping as high as possible the power efficiency.

In many DC-DC converters applications [1]-[3] there is an external diode to charge the bootstrap capacitor and an external power transistor to supply the load. These external components increase the PCB size. To reduce the size of external components, it is necessary to eliminate the problems related to the switching speed deriving from the driver and from the level shifter. Thus, for these blocks it is necessary to develop new solutions as those here proposed that fully integrates such external components. In fact, the power transistor [4] and the block used to charge the bootstrap capacitor have been integrated on silicon, allowing to minimizing capacities, inductances and resistances in the PCB. The aim is increasing the gate drive frequency up 1MHz, with high dV/dt for V_{DS} on power transistor. The proposed gate driver, bootstrap circuit and level shifter is designed for a load that requires a constant current of 2.9A with an input voltage range of 4.5V to 27V.

The paper is organized as follows. The gate driver and the other blocks are presented in Section II. The simulation results are given in Section III, and Sections IV concludes the paper.

II. Architecture and Operation

A. Gate driver Architecture

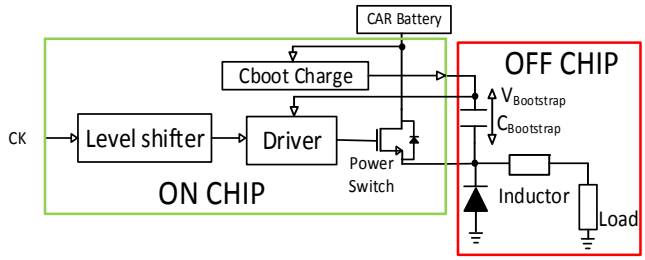

Fig. 1 Block diagram of gate driver

The structure of the proposed on-chip HV gate driver in an asynchronous buck converter is shown in Fig. 1. There are different blocks: the dead time generator, the level shifter, the inherent bootstrap charge, and the driver. $V_{bootstrap}$ is a floating voltage that can range from below ground to above battery voltage. In the next section, the operation of each block will be explained.

B. Dead Time Generator

The Dead Time generator is the Timing Control (TC) block that provides an appropriate dead-time between the switching on and off of the power transistor. The Dead Time generator is used to produce for the level shifter two signals: one signal turns on the switch (ck_{low}) and the second one turns it off (ckq_{low}). Between the two signals a dead time to avoid overlapping of the on and off state is inserted.

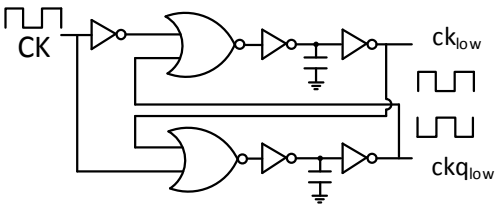

Fig. 2 Dead Time generator

Referring to analog solution of Fig.2, the non-overlapping time is defined by means of two capacitors of the same value. The capacitances are sized (2pF) to obtain approximately 20ns of non-overlapping time. The 20ns is the maximum fall time to switch on the power transistor. The analog solution, for this technology, reduces the die area compared to the digital version.

C. Level shifter

The level shifter transfers a signal from the low voltage (low side) domain, into the high voltage domain of the output stage. Among are different possible solutions, for low frequencies, the scheme in Fig. 3 can be used e.g. with three diodes to transmit the signal from the low voltage domain to the high one. However, this structure features high power consumption for high frequency operations.

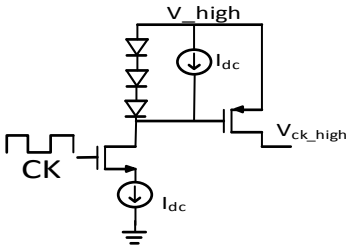

Fig. 3 Level Shifter for low speed applications

In this design the scheme of Fig. 4 is preferred, which is based on low and high voltage transistor. The transistors M1 and M2 are high voltage. The remaining transistors are instead low voltage, because the difference between $V_{bootstrap}$ and V_S (voltage source on power switch) will be limited by design.

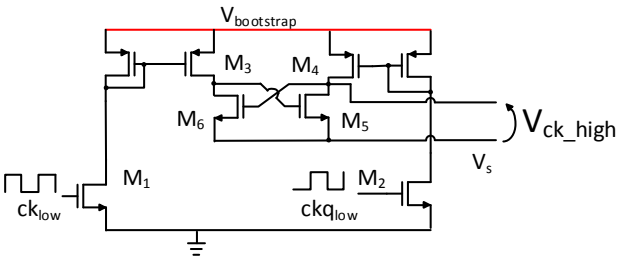

Fig. 4 Level Shifter

This level shifter operates with a floating supply voltage, indeed $V_{bootstrap}$ is above the battery voltage when the power transistor turns on. Two complementary clocks (ck_{low}, and ckq_{low}) generated by the Dead Time generator are used to drive this structure. Between the two signals, there is a dead time to stabilize the level shifter, preventing a non-switching due to excessively high frequency. When clock ck_{low} is high, M1 is turned on and M2 is off, in the first branch there is a current and therefore M3 turns on and the voltage on $V_{D(M3)}$ is shows in Eq. 1.

$$V_{D(M3)} \approx V_{bootstrap} - V_{DS(M3)} \quad (1)$$

as a consequence, the transistor M5 turns on, because

$$V_{D(M3)} > V_{th(M5)} \quad (2)$$

while M6 turns off. Hence, when the ck_{low} is high, the V_{ck_high} is a digital zero and vice versa when ck_{low} is low. By means of the inverter, the output signal is synchronous with the input signal on M1. The delay between input and output can be kept in order of 6.4ns enabling high speed operations.

D. Power switch

The choice of the power transistor dimension depends on the switching frequency and the associated losses. Fig. 5 shows the losses related to a power transistor with an $R_{ds(on)}$ equal to 150mOhm and that of a transistor with an $R_{ds(on)}$ equal to 50mOhm. As the switching frequency increases, turns out that the capacitive losses are more relevant than the conduction losses. For low frequency, instead, the power losses are proportional to the switch resistance. Therefore, a small power transistor 150mOhm is preferable when the frequency increases. As a consequence, also the area consumption reduces.

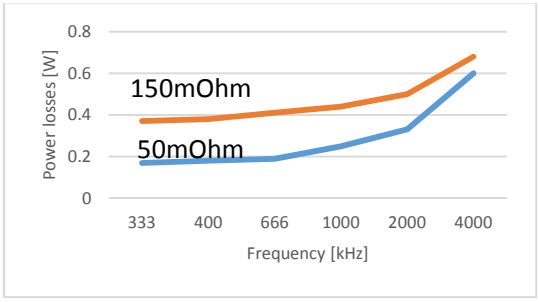

Fig. 5 Power losses on power switch vs frequency

E. Gate Driver

The gate driver in Fig. 6 determines the state of the power MOSFET. The gate driver is composed by a pair of low voltage MOSFET and it is designed to pilot a power transistor.

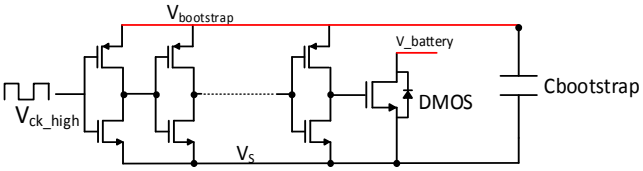

Fig. 6 Gate Driver

The delay between the input signals and the output signal for a driver is negligible.

Since a NMOS offers higher mobility than a PMOS, it is convenient to use the NMOS as high side power in terms of implementation area (while providing the same on-resistance during conductions). Because of the high frequency operation requirement, the higher ohmic power transistor of Fig. 5 has been selected. To design a fast switching on-chip gate driver, the equivalent gate capacitance of the power transistor has been calculated (C=1nF). From the basic equations below:

$$Q = C * \Delta V \quad (3)$$

$$Q = I * \Delta t \quad (4)$$

where Q is the equivalent charge, ΔV is the maximum V_{GS} on power transistor, Δt is the rise time of V_{DS} and I is the average gate current to charge the equivalent capacitor. Once the rising time, is set the above equations are rearranged to obtain the average current to switch:

$$I = \frac{C*\Delta V}{\Delta t} = 300mA \quad (5)$$

Moreover, to design the last branch of the gate driver it was made the following approximation:

$$\Delta t = 3 * \tau = R_{on_{pmos}} * C \quad (6)$$

$$R_{on_{pmos}} < 10\Omega$$

To guarantee a secure margin, $R_{on_{pmos}}$ is designed to be 2Ω. Moreover, during simulations W/L=48 with multiplicity equal to 100 has been used (Fig. 6) and for the $R_{on_{nmos}}$ the ratio is 2.5 times smaller.

F. Bootstrapping technique for driving the n-type high-side switch

This circuit recharges the external bootstrap capacitor. The capacitor has been used to generate a voltage turning on the power switch. For high frequency, this system is faster than the charge pump.

The bootstrapping scheme is illustrated in Fig. 7. When V_s assumes a ground voltage (considering the schottky diode as ideal, i.e. with 0V forward voltage drop during conduction), the bootstrap capacitor is charged to a value $V_{bootstrap}=I_{dc}*R_{ref}$. The switch M2 inside the level shifter (Fig. 4) turns off, while M1 must be turned on, and the voltage across the bootstrap capacitor acts as a temporary supply voltage for the level-shifter and as a buffer for power transistor. As soon as the power transistoris switched on, its source voltage is pulled up as well as the auxiliary supply voltage level $V_{bootstrap}$ because of the the bootstrap capacitor. Note that the parasitic diode of the HV NMOS becomes reversely biased since the bulk terminal is always biased such that its voltage is below the input one. Afterwards, the bootstrap capacitor slowly discharges through the level-shifter and the buffers. However, its capacitance is large enough to maintain a sufficient charge until the switch turns off again. Furthermore, from Fig. 4 shows that the V_{ck_high} may exceed of few volts the battery voltage, which is approximately the value reached by the Vs node minus the voltage drop on power transistor. This scheme allows to charge the bootstrap capacitor with switching frequencies >1MHz, because the capacitor starts to charge when the voltage bootstrap is one Vth_{MHV} lower than the voltage battery.

To charge the bootstrap a current coming from a bandgap reference is used. This compensated current is necessary to make the bootstrap voltage insensitive to temperature variation. Due to the M_{HV} body effect, its threshold increases leading to Vbootstrap inaccuracy (the reference voltage will be the sum of $V_{bootstrap}$ and Vth_{MHV}). To have the same voltage between the $V_{bootstrap}$ and the node above R_{ref}, a diode-connected transistor it is used to compensate the V_{GS} drop over M_{HV}. M_{HV} is chosen to be a high voltage transistor to avoid breakdown since the capacitor is directly connected to the input voltage. Indeed, the voltage drop on M_{HV} can be higher than 25V in the worst case. The right bootstrap capacitance must be selected according to the application by mean of this formula:

$$C_{bootstrap} \geq \frac{Q_{tot}}{\Delta V_{bootstrap}} = \frac{3nC}{0.4V} = 7.5nF \quad (7)$$

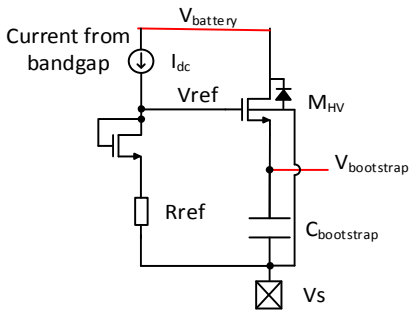

Fig. 7 Bootstrap circuit

III. Simulation Results

The proposed HV asynchronous gate driver hereby presented requires few nanoseconds to switch the power transistor. It also provides a built-in high-side supply with only one off-chip coupling capacitor, thereby offering a strong driving capability for high-side power NMOS. Fig. 8 shows the load current of 2.9A and the power transistor voltage drop for 12V of input voltage in standard conditions for car battery. The duty cycle is the 33% of the period.

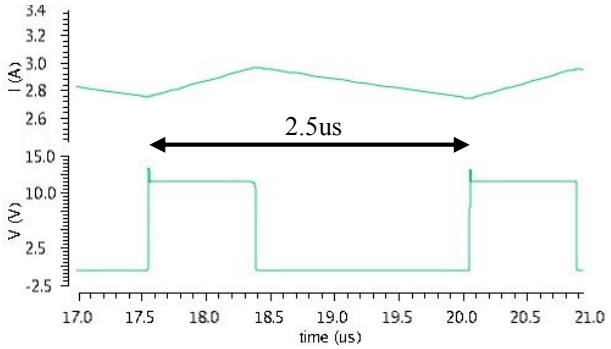

Fig. 8 Load current, V_{DS} on power transistor, f_{sw}=400kHz

In Fig. 9 the V_{DS} drop on the power switch (upper plot), and the V_{GS} drop (lower plot) using 1MHz switching frequency are shown. It results that the frequency increase doesn't affect the falling time and the rising time. The system is well optimized, achieving fast switching when dealing with high current.

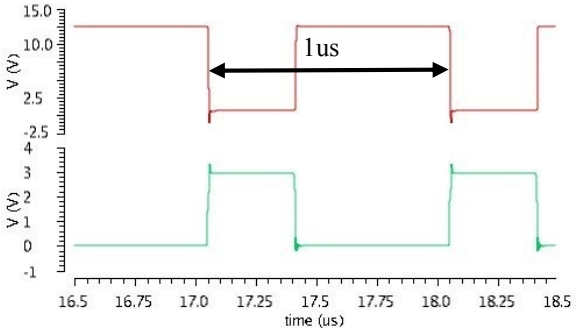

Fig. 9 V_{DS} on power transistor, V_{GS}, f_{sw}=1MHz

The power transistor variation dV/dt during the rising time is 6.35V/ns, while it is 3.55V/ns during the falling time.

In Fig. 10 and Fig. 11, the power transistor falling and the rising time on the V_{DS} are shown.

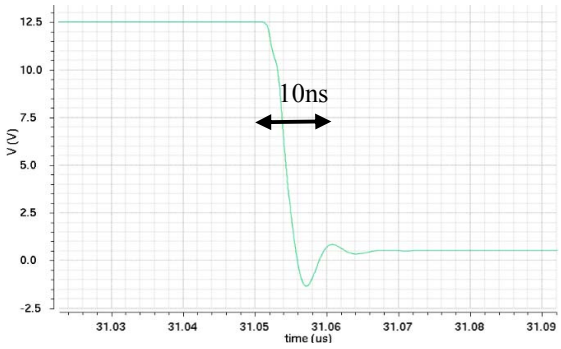

Fig. 10 V_{DS} voltage drop, falling time

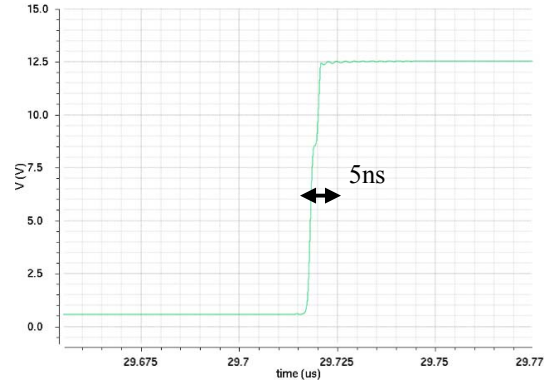

Fig. 11 V_{DS} voltage drop, rising time

With this type of structure for the gate driver, the efficiency of the integrated circuit without considering the external components reaches 94.4%. In Fig. 12 shows the layout.

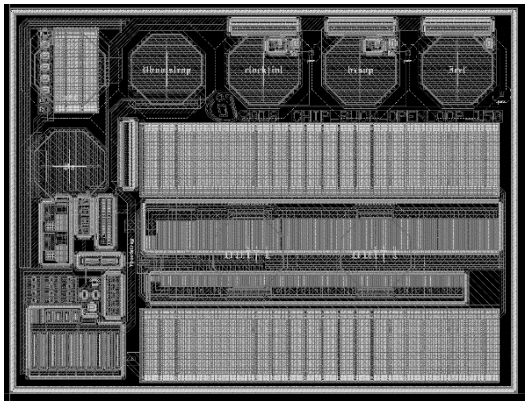

Fig. 12 Gate driver with on-chip power switch

A. Comparison

Table I shows the comparison between the state-of-the-art solutions and the presented work. The used external components are: Schottky diode, 30uH inductor and a load requiring 2.9A constant current.

IV. CONCLUSIONS

In this paper a high voltage on-chip gate driver was presented. The designed level shifter structure allows a rapid state transition of the high-side switch. The monolithic circuit has an efficiency of 94.4%, not including the losses due related to the used external components. The efficiency with the external components is 80.17%, in fact the limitation derives from the quality of external components. Another advantage comes from the low-cost technology involved in the design. Consequently, the circuit reaches high efficiency even in a high frequency regime, without giving up a competitive price for the final product.

TABLE I. PERFORMANCE COMPARISONS OF DIFFERENT BUCK CONVERTERS

	Comparison			
	LTC3630 [5]	***LM5007 [6]***	***LM5017 [7]***	***This Work***
Converter topology	Synch. Buck	Async. Buck	Sync. Buck	Asynch. Buck
Input Voltage (V)	12.5 - 76	12 - 75	12.5 - 95	4.5 - 27
Fsw (kHz)	N. A.	400	200	500
Output voltage (V)	12	10	10	3.5
Max Output Current (A)	0.5	0.4	0.6	3.5
Efficiency	92% at Vin = 24V	93.7% at Vin = 15V	92.5% at Vin = 24V	80.17% at Vin = 12V [a] 94.40%

[a.] Driver efficiency

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