Variable off-Time Peak Current Mode Control (VoT-PCMC) as method for average current regulation in Buck Converter Drivers(*)

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***Abstract*—In automotive industry, every electronic device is driven by power switches. Indeed, the energy source is the car battery and it cannot, for instance, limit the output maximum voltage level. Consequently it could be higher than that supported by the load. The DC/DC Buck converter acts by limiting the output variables, according with the load specifications thereby ensuring its correct operation. The overall circuit will be composed of a power stage, the basic DC/DC converter, and a control loop, to provide a target output current value. This paper presents a control algorithm derived from an improved Peak Current Mode Control. The proposed algorithm defined Variable off-Time Peak Current Mode Control (VoT-PCMC) allows to contemporarily control in a DC-DC converter the ripple and the average current values, leading to a reliable load driver. The algorithm operation is simulated and then tested on hardware using dSpace, a Rapid Control Prototyping set-up.**

Keywords—DC/DC Converter, Buck Converter, Peak Current Mode Control, Simulink, dSpace, Automotive

I. INTRODUCTION

Demand of integrated converters is increasing over conventional ones. Integrated circuits must taking up small space and having the fewest external components for cost reduction. The energy conversion efficiency is another main aspect to achieve greener and greener solutions. Automotive electronics operating from car battery experience transient voltages such as cold-cranking and load dump, which can range from 4.5V to >27V. In addition, systems such as start-stop increase the frequency of these transients and operational requirements of electronic devices. Off-battery power ICs are therefore needed to withstand harsh operating conditions and reliably provide power to the whole vehicle. The proposed control algorithm may be applied to a very flexible DC/DC converter with a wide input voltage range ([4.5, 27]V). An application case could for instance be a LED driver. In order to get an efficient and reliable driver, a feedback loop is needed to align the current features, i.e. the peak, the mean and the ripple, with those required by the load specifications. Various solutions for the feedback loop have been proposed in literature, as in [3]. The Peak Current Mode Control (PCMC), compared to other methods, seems to be the most advantageous in terms of:

- simplicity of the loop (low manufacturing cost) without the need for a compensator;
- quick recovery of the regulation;
- sampling advantages, since the output current reading can be limited to the on-switching phase and not extended to the entire period (low power consumption);
- further improvement, to reach more accurate and reliable solutions, are available.

However, the PCMC presents many drawbacks, including instability issues, generally solved with the Slope Compensation technique. On the other hand, the Variable off Time PCMC (VoT-PCMC) is here proposed improving the basic solution and solving all drawbacks by allowing the off-switching period (t_{off}) to change at each switching cycle accordingly to the output current target.

The presented algorithm has been applied to a circuit that supplies an average output current of 3A±5%, maintaining at the same time the peak below 3.5A, thus indirectly limiting also the ripple. Approximating the load as a linear component, a 1.5ohm resistor was used to test the functionality of the circuit.

The paper is organized as follows. The basic principle and laws of the Buck DC/DC converter are presented in Section II. The design and structure of the control circuit are described in Section III. In Section IV the results of the simulation system using dSpace are discussed, finally followed by the conclusion in Section V.

II. WORKING PRINCIPLE

A. Buck Converter

Fig.1 shows the basic Buck converter schematic. Usually there is also an output capacitor, C_L, to reduce the output voltage ripple. Since the main goal is to control the output current, the output voltage, V_{out}, can be left with no directly

(*) Patent pending [1]

control and dependent on the load (temperature etc.). The C_L can therefore be neglected leading to a cheaper system.

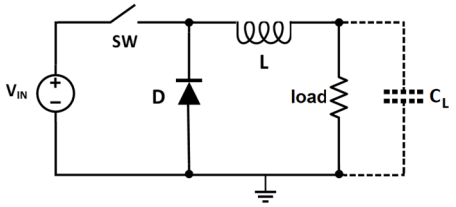

Figure 1: Buck basic circuit

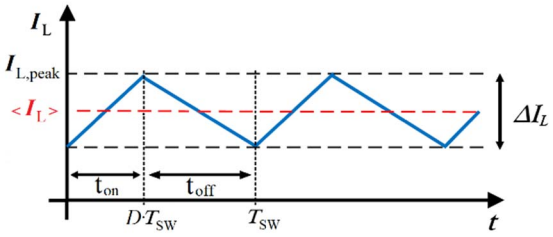

Figure 2: Output current waveform

The main equations controlling the Buck converter operation are shown below. First of all, the relation between the output voltage, V_{out}, and the input voltage, V_{in} is:

$$\boldsymbol{V_{out} = D \cdot V_{in}} \quad (1)$$

where the Duty Cycle, D, is defined as follow:

$$D = \frac{t_{on}}{T_{SW}} = \frac{(T_{SW} - t_{off})}{T_{SW}} \quad (2)$$

The period T_{SW}, i.e. sum of t_{on} and t_{off}, varies with the output voltage, the input voltage and the inverse of the inductance value L. From (1) and (2), t_{off} is given by:

$$t_{off} = \left(1 - \frac{V_{out}}{V_{in}}\right) \cdot T_{SW} \quad (3)$$

Taking the product between the current flowing rate through the inductor during the off-switch phase (i.e. diode on) and the t_{off} value, the current ripple ΔI_L is obtained as:

$$\boldsymbol{\Delta I_L = \frac{V_{out}}{L} \cdot t_{off}} \quad (4)$$

This equation is also used to relate the t_{off} value to the current average value, $< I_L >$, by means of the peak current value, $I_{L,peak}$, indeed:

$$\boldsymbol{< I_L >= I_{L,peak} - \Delta I_L/2} \quad (5)$$

In order to drive a load, e.g. a LED for lighting application, these current features must be controlled.

B. Current Sensing

The first step in the control is reading the current value. The read value is then fed-back into the control loop where, for example, it is compared to a reference value. On the basis of that comparison, the loop will act on the switching activity (turning on/off the switch to provide more/less current). Fig.3 shows the Simulink schematic of the Buck converter with a shunt resistor, *Rsense*, used to measure the output current. Usually, it is either connected in series to the inductor or connected to the output load. However, this would lead to higher power consumption since the sensing would take place both in the on-switching phase and in the off one. On the other hand, PCMC algorithm reads the current only during the on-phase. Therefore, it is preferable to interpose *Rsense* between the switch and the diode, avoiding Joule effect losses during the off-switching phase.

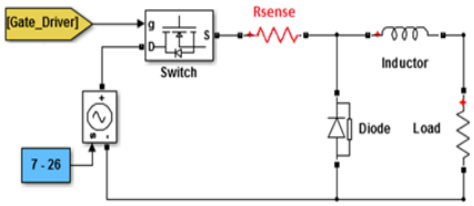

Figure 3: Buck schematic on Simulink

C. Control loop

The basic Buck converter cannot drive the target load without a proper current control loop. Different control loop solutions are available, but only few ones guarantee the highest reliability together with low production cost, like the PCMC, as shown in Fig.4 (left) whose basic operations are in Fig.4 (right). The sensed output current, I_{sense}, is compared with a peak reference, I_{ref}. Once I_{sense} reaches the reference, the switch is turned off by means of a SR latch to avoid exceeding the maximum prefixed value. As a result, the system is intrinsically protected against over-currents and short circuits. After a certain period, T_{SW}, (chosen by the user in line with efficiency/cost requirement of the chip) the switch is then reactivated, returning a triangular output current waveform.

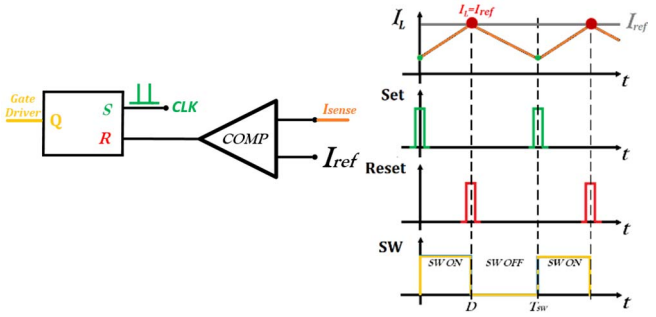

Figure 4: PCMC control loop (left) and operation (right)

A basic PCMC loop controls only the maximum current flowing into the load, leaving the ripple and the average current values free to change. Therefore, such a solution is not reliable in those applications where the load can only support tiny shifts around a given current average value/ small current ripples. Furthermore, the worst problem is yet to come and concerns the system stability whenever the duty cycle is >50%. If, for example, the load is 1.5ohm and the V_{out} is 4.5V, instability arises whenever the V_{in} is <9V.

III. Variable Off-Time PCMC (VoT-PCMC)

To overcome instability and to improve the PCMC reliability, subsequent improvements have been made that led to the VoT-PCMC. The control loop concept is based on increasing/decreasing the t_{off} value depending on the difference between the calculated $< I_L >$ and the target average value. For instance, if $< I_L >$ is higher than the

desired value, the t_{off} value will be raised to increase the ripple and consequently decrease the average (from (5) and (6)).

Fig.5 shows the Simulink (MATLAB) control loop implementation. The lower part is composed by a comparator, a SR latch and a counter (*CLK*), as it was for the basic PCMC. The current is read (*Isense*) and compared with a peak reference. Whenever *Isense* is higher, the switch is turned off through the Reset of the SRlatch and the counter starts counting from zero up to a value t_{off}. The switch is then turned on again via the Set input.

The t_{off} value is imposed by the upper part of the control circuit, composed by: a register, a mean calculator, an error calculator and an adder. When the switch is turned on, the inductor current is at its minimum value. By providing a link between the Set signal and the Enable of the register a sample&hold results. Thereby the register stores and updates the minimum current value each time the Set is activated. The mean calculator is then used to calculate the current average value. Next, an error calculator compares that value with the desired average (*Imean*, in purple) and returns the percentage error with sign:

$$error\% = \left[\left(\frac{I_{ref} - I_{sense,stored}}{2}\right) - I_{mean}\right]\frac{100}{I_{mean}} \qquad (6)$$

This error will be finally summed to the previous t_{off} to get the increased/decreased new value.
Using a percentage error is an efficient solution since the t_{off} changes rapidly whenever the calculated average is far from the desired value, while it changes slowly otherwise. Overshoot and ringing on the t_{off} value are then minimized.
Fig. 6 shows a flowchart with the purpose of reproducing the entire system algorithm just illustrated.

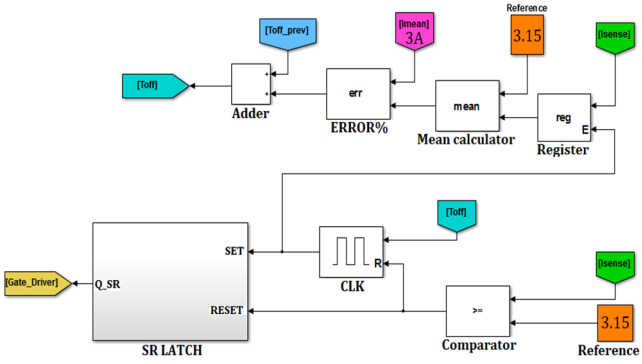

Figure 5: Control circuit Simulink schematic

IV. Laboratory Set-up

The circuit was firstly simulated under ideal condition with Simulink (MATLAB) and then it was tested in the laboratory using a real switch and a real load. Fig. 7 shows the laboratory set-up block diagram. The emulator dSpace provides the connection between the PC and the converter hardware, shown in Fig.8. In particular, dSpace contains an FPGA on which the control circuit is uploaded, after being automatically translated by Simulink and coded in VHDL. In fact, dSpace embodies the control circuit to be tested. Afterwards, a Graphical User Interface (GUI) allow the user to check the hardware responses. For instance, in the VoT-PCMC, the output current is read from the DC/DC PCB and sent through the ADC to the FPGA, where the current control will be performed as described above.

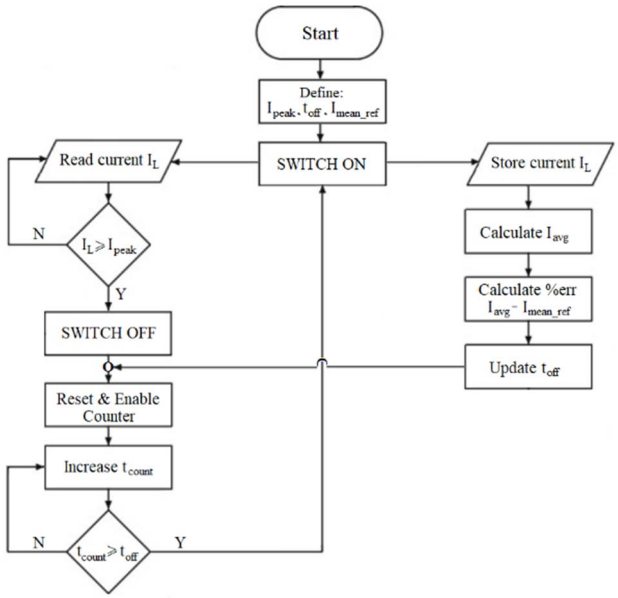

Figure 6: Control circuit flowchart

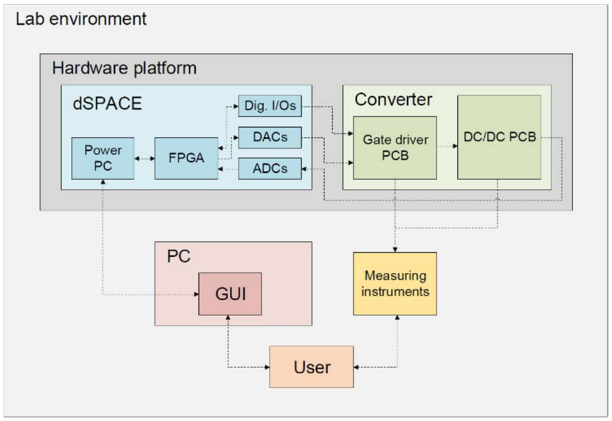

Figure 7: Laboratory environment

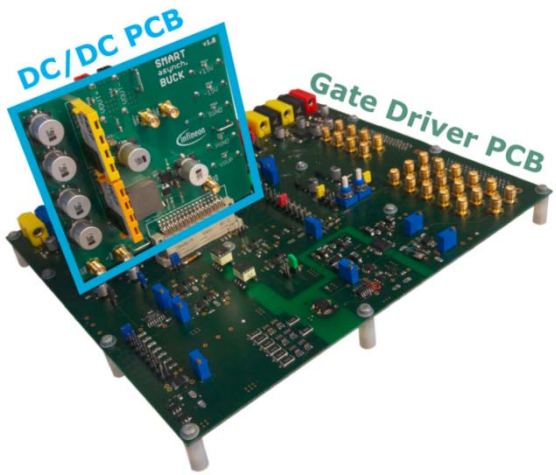

Figure 8: Converter hardware

V. Experimental Results

In nominal condition, the current waveform obtained for a V_{in}= 16V is shown in Fig.9. Instability is solved as proved in Fig.10 where a sudden change in the Vin (from 18V to 7V) is simulated, raising the duty cycle >50%. In addition, the line-to-output rejection is extremely satisfying.

TABLE 1: Comparison between the control methods

Control method	HCMC	PCMC	ACMC	PCMC +Slope comp	VoT-PCMC
Loop simplicity	++	++	-	+	+
Current regulation precision	-	-	+	+	++
Noise immunity	-	-	++	+	++
Reference perturbation	-	+	++	+	++
Line perturbation	+	+	+	++	++
Rapidity	++	++	-	++	++
Sampling advantages	-	++	-	++	++
Stability	++	-	++	++	++
Improvement available	-	++	-	-	-

Once reached a steady state condition, Fig.11 shows the response when a perturbation of the peak reference (positive step up to 3,5A @ 16V, *Imean*=3A) is added. As expected, to keep $< I_L >$ close to the $< I_L >$, the control loop increases t_{off}. Fig.12 shows instead how the system reacts to an average reference perturbation (positive step up to 3.15A @ 16V input voltage, *Ipeak*=3.4A). The loop gradually reduces the t_{off} value to increase $< I_L >$, making it closer to the new reference.

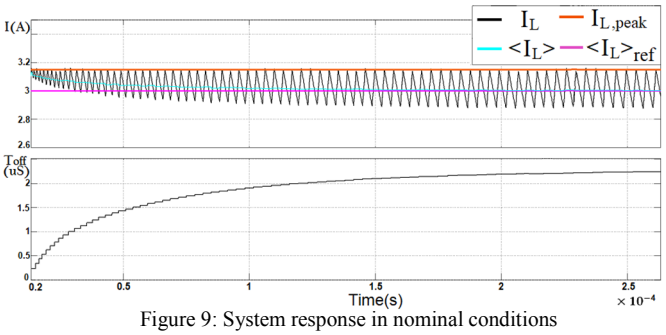

Figure 9: System response in nominal conditions

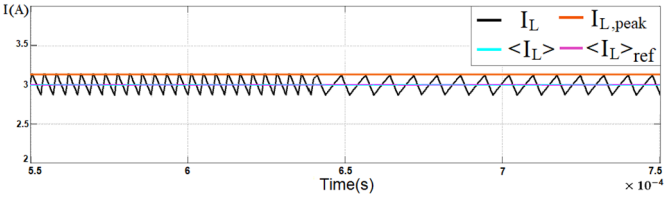

Figure 10: Response to negative input voltage step

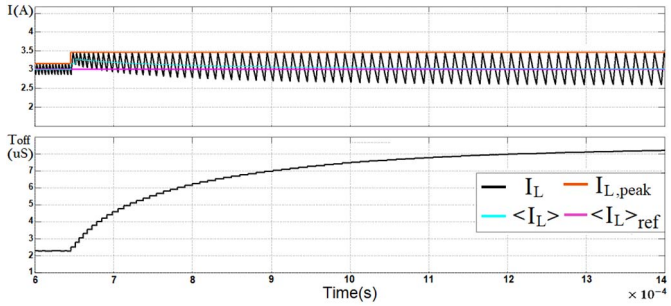

Figure 11: Response to a peak reference positive step

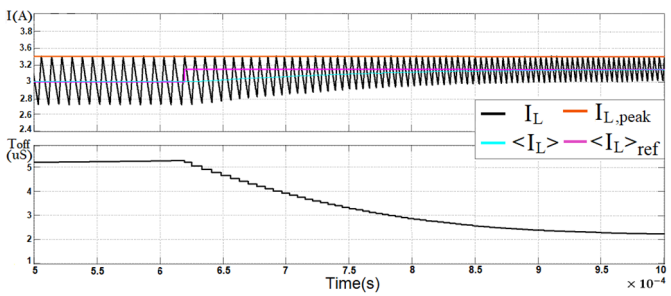

Figure 12: Response to an average reference positive step

VI. Conclusions

Starting from the basic PCMC, the VoT-PCMC has been developed and proposed. The VoT-PCMC ensures an optimal control of all current features, without any stability issues. Indeed, with a variable frequency is no longer required any additional repair technique such as the Slope Compensation.

Tab.1 summarizes the distinction with the most common control methods to empathize the performance and design advantages of the presented solution compared to the state of the art.

Contrarily to [7], the design foresees the absence of the Buck capacitor and a 30uH inductance. The system works with an input voltage range of [4.5,27]V and it is able to drive a single future 3A LED with a maximum switching frequency of 500kHz, allowing extremely good average regulation precision and speed.

Finally, the worst case simulations adding overstated perturbation were shown. These prove that in fact the VoT-PCMC shows extremely good responses in all conditions.

VII. Acknowledge

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