DC-DC Buck Converter with Constant Off-Time Peak Current Mode Control

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***Abstract*—The paper presents an upgrade of the Peak Current Mode Control (PCMC) for a Buck DC-DC Converter. Constant Off-Time algorithm has a fixed off-switch phase, and, conversely to the typical PCMC, the duration of the switching period is free to change depending on the load and the battery voltage. In this way the instability issues, typical of a PCMC, are solved. The circuit is able to robustly sink $3 \pm 5\%$A average current from a car battery source, in a 3.5 V output voltage - 212kHz maximum frequency application. In addition, the circuit intrinsically provides protection against over-current and allows precise control over the current features (peak, average and ripple). The concept will result in a fully integrated system without external pad to sense the current, thanks to the proposed integrated sensing technique. The power consumption is also reduced since the current is read only during the on-switch phase.**

***Index Terms*—DC-DC, Buck Converter, Constant Off-Time, Control loop, Peak Current Mode Control**

I. Introduction

In Automotive industry, electronics devices operate from car battery which can range from 4.5V to 27 V. DC-DC converters are used to source them insuring their correct operation and protection against over-current and over-voltage.

In this paper, an improvement of the Peak-Current-Mode Control (PCMC) operating in Continuous Conduction Mode (CCM) with a Constant Off-Time (Constant-T_{off}) is presented. The control loop allows the DC-DC Buck converter to reliably drive a constant load by controlling the output current [2], [3]. Instability issues related to a fixed switching frequency [7] are intrinsically solved as well as over-current issues (indeed the maximum current is fixed). This avoids the use of techniques such as Slope Compensation [8], which increase the complexity of the system moreover without ensuring a satisfactory precision in controlling the current features. The proposed system operates with 212kHz maximum switching frequency, delivering a 3A average current with a 3.5V load-fixed output voltage. The PCMC algorithm is embodied in the power supply system on a battery driven integrated CMOS circuit without external pad to sense the current, resulting in a lighter circuit. Moreover, compared to the most common solutions [5], [6], the here used fully-integrated Current Sensing solution requires less external components, with consequent lower cost in terms of BoM and board fabrication.

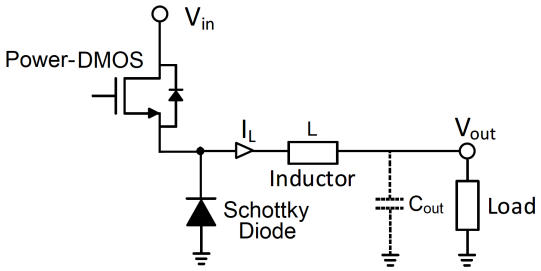

Fig. 1. Buck converter scheme

The paper is organized as follows. The algorithm principle is presented in Section II. Section III describes the DC-DC Buck converter architecture. A comparison with the state of the art is given in Section IV. The simulation results are shown in Section V and the conclusions are drawn in Section VI.

II. Constant-T_{off} PCMC Algorithm Operation

A DC-DC Buck converter is a device which converts its input voltage to a lower output voltage by repeatedly turning on and off a power switch (Power-DMOS). A conceptual scheme of a DC-DC Buck converter is given in Fig. 1.

Two phase are identified: the ON-phase when the Power-DMOS conducts (T_{on}) and the OFF-phase when the diode conducts (T_{off}). Referring to the Duty-Cycle (D):

$$\begin{cases} T_{on} = D * T \\ T_{off} = (1-D) * T \quad with \quad T = T_{on} + T_{off} \end{cases} \tag{1}$$

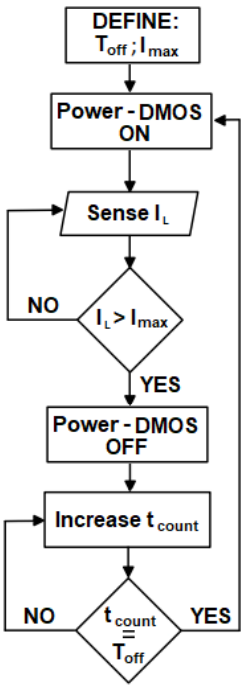

Fig. 2. Constant-T_{off} PCMC algorithm flowchart

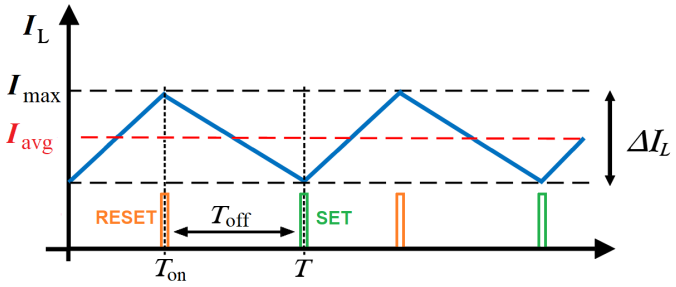

Fig. 3. Output current

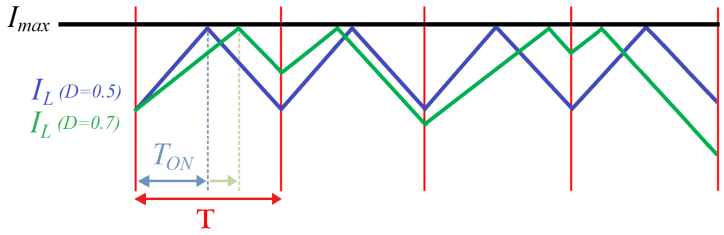

Fig. 4. Output current in typical PCMC

In the application at stake, the load fixes the output voltage V_{out}, provided that a certain current I_L (equal to the inductor current) is properly driven through it. The typical output filter capacitor (dotted in Figure 1) is therefore no longer needed. The load works with an optimum average current I_{avg} and the current, to avoid damages, must be lower than a maximum I_{max}. The current ripple ΔI_L is then:

$$\Delta I_L = 2 * (I_{max} - I_{avg}) \tag{2}$$

In standard PCMC, the period T is fixed and the T_{off} is variable, conversely to the proposed Constant-T_{off}. The flowchart in Fig. 2 resumes its operation.

During T_{on}, the load current increases with a positive slope:

$$\left(\frac{dI_L}{dt}\right)_{ON} = \frac{\Delta I_L}{T_{on}} = \frac{V_{in} - V_{out}}{L} \tag{3}$$

When I_L reaches I_{max}, the OFF-phase starts and the output current decreases with a negative slope:

$$\left(\frac{dI_L}{dt}\right)_{OFF} = \frac{\Delta I_L}{T_{off}} = -\frac{V_{out}}{L} \tag{4}$$

After a time T_{off}, the DMOS is turned ON again and the system keeps on operating. The resulting triangular current waveform is that of Fig. 3.

T_{off}, from (4), is constant and load-dependent, while T_{on}, from (3), changes also with the battery voltage:

$$T_{on} \propto \frac{1}{V_{in} - V_{out}} \tag{5}$$

From (3) and (4) it is derived that:

$$(V_{in} - V_{out}) \cdot T_{on} = V_{out} \cdot T_{off} \tag{6}$$

Which gives, from (1):

$$V_{in} \cdot T_{on} = V_{out} \cdot T \Rightarrow \frac{T_{on}}{T} = \frac{V_{out}}{V_{in}} = D \tag{7}$$

The T_{off} choice depends on the maximum power-DMOS frequency (f_{max}). Based on the above considerations, f_{max} can be evaluated for T_{on} tending to zero, therefore:

$$f_{max} = \frac{1}{T_{off}} \tag{8}$$

A typical PCMC is inherently unstable when D> 0.5 [7] (i.e. $T_{on} > T_{off}$ or equivalently $V_{out} > V_{in}/2$ from (7)). If $V_{in} = [4.5, 27]$ V and $V_{out} = 3.5$ V, the system would be unstable for $V_{in} < 7$V. Fig. 4 empathises the difference between the limit case $D = 0.5$ and the unstable case $D = 0.7$. Indeed, in typical PCMC, after a fixed period T, the power-DMOS turns ON. While, in Constant-T_{off}, the power-DMOS turns ON T_{off} seconds after the current has peaked. At that time, the current will necessarily be: $I_{max} - \Delta I_L \cdot T_{off}$ (here the ripple is fixed). If T_{on} changes, accordingly to the input voltage, the switching frequency will also change, without impacting the current features. Thus, techniques as Slope compensation [4] to insure stability are no longer needed.

III. Constant-T_{off} Algorithm Implementation

Only two external components needed: the inductor (L) and the Schottky Diode. The main blocks, according to Fig. 5, are: the Current Sensing, the Control Logic blocks, the Protection, the Internal Reference (including a bandgap voltage reference to generate V_{max}, related to I_{max}), the gate Driver to turn on and off the Power-DMOS and the Power Supply to generate a low voltage domain for the low side circuit.

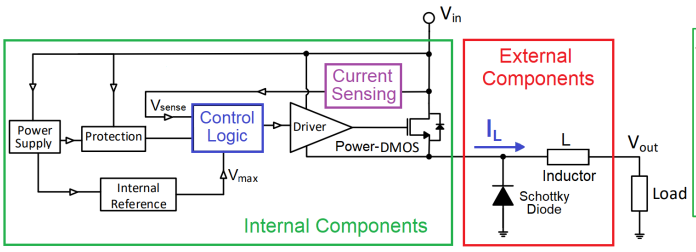

Fig. 5. Top level Schematic

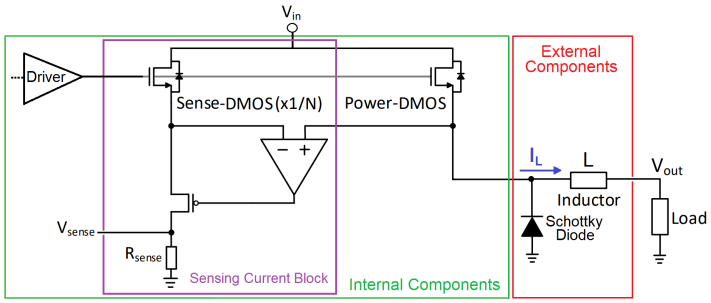

Fig. 6. Current Sensing block diagram

A. Current Sensing block

As shown in Fig. 6, the current sensing is implemented using a matched Sense-DMOS with a $N = 1/1000$ mirroring factor to minimize power consumption in the Sense branch. The OpAmp forces the drain-source voltages of both switches to be equal such that I_{sense} is $1/N = 1/1000$ smaller than I_L. I_{sense} flows through R_{sense} to generate V_{sense}, which will be a comparator input of Fig. 7. Power consumption is reduced w.r.t other external current sensing techniques since the proposed Sensing technique only operates during the ON-phase. During the OFF-phase, indeed, no current flows in the Sense branch. Due to the large Power-DMOS current and its layout proximity to the Sense-DMOS, a significant temperature gradient could arise, affecting the maximum current value. Moreover, due to the resistor temperature coefficient, the V_{sense} could vary. However, if V_{max} (Fig. 7) is generated by means of the I_{max} reference and a resistance R_{max} (same type as R_{sense}), the temperature effect is canceled, making the system temperature-independent.

B. Control Logic block

Fig. 7 shows the Control Logic block implementation. The result of the comparison between I_{sense} with I_{max} gives the Reset of the SR Latch. When $I_{sense} \geq I_{max}$, the Reset activates and the Power-DMOS turns OFF thorugh the gate driver. The Set input is instead connected to a counter. As soon as the Power-DMOS turns off, the counter starts counting up to T_{off} duration. Afterwards the Set is activated and the Power-DMOS turns ON. As long as the current is lower than I_{max}, the counter does not count (since the SR-Latch output is a logic '1', connected to the counter $Reset$).

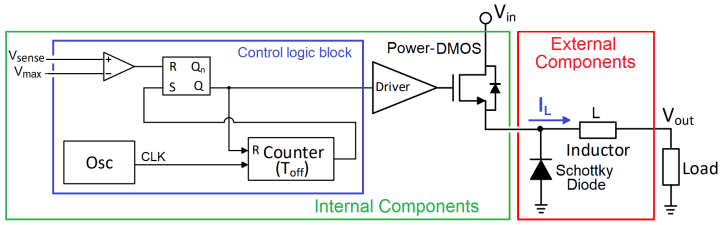

Fig. 7. Constant T_{off} Current Control Loop implementation

IV. Comparison with State-of-the-Art

A valid alternative is the Variable-T_{off} PCMC [1], where, other than the current peak, also I_{avg} is controlled. Here, the T_{off} period increases/decreases at each switching cycle accordingly to the comparison between I_{avg} and the desired value, making (2) smaller/bigger (i.e. increasing/decreasing I_{avg}). The f_{sw}, beside changing with the input voltage, will also depend on the T_{off} value. Nevertheless, in Variable-T_{off}, the current ripple is not directly controlled, but rather fixed by the peak and average values. Compared to the proposed Constant-T_{off}, Variable-T_{off} is more precise in controlling the average, but more complex and with a very variable f_{sw}. On the other hand, Constant-T_{off} accurately controls the peak and the ripple. Consequently, also the average current value is indirectly controlled. Both algorithms solve the instability issues of a basic PCMC, returning reliable and precise circuits.

V. Design Example and Simulations Results

Table I resumes the application specs.

TABLE I
CIRCUIT SPECIFICATIONS

Technology	0.35 μm
V$_{in}$	4.5-27 V
V$_{out}$	3.5 V
f$_{max}$	212 kHz
Maximum Current Level	3.3 A
Average Current Level	3 A
Output Current Ripple	0.60 A

From (8) the upper T_{off} limit is obtained:

$$T_{off} < \frac{1}{212kHz} = 4.7\mu s \tag{9}$$

In fact, $T_{on} \neq 0$ and T_{off} will be slightly lower than (9) to fully exploit the Power-DMOS operative frequency range. The highest frequency corresponds to the lowest T_{on}, i.e the highest V_{in} (5). Since $1/f_{max} = T_{on,min} + T_{off}$, (6) becomes:

$$V_{out} * T_{off} = (V_{in,max} - V_{out}) * (1/f_{sw,max} - T_{off}) \tag{10}$$

Therefore:

$$T_{off} = \frac{27V - V_{out}}{27V} * \frac{1}{212kHz} = 4.1\mu s \tag{11}$$

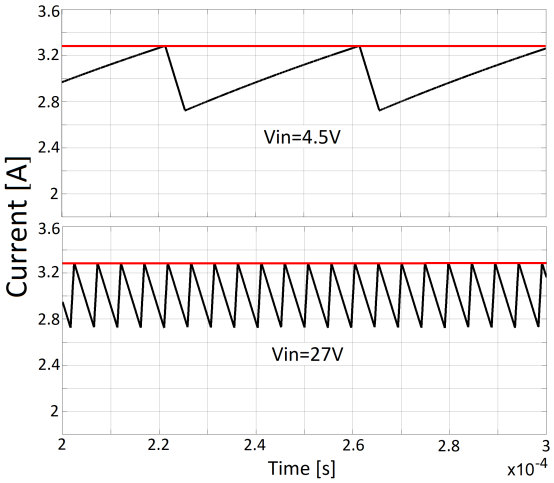

Fig. 8. Load current waveform varying V_{in}

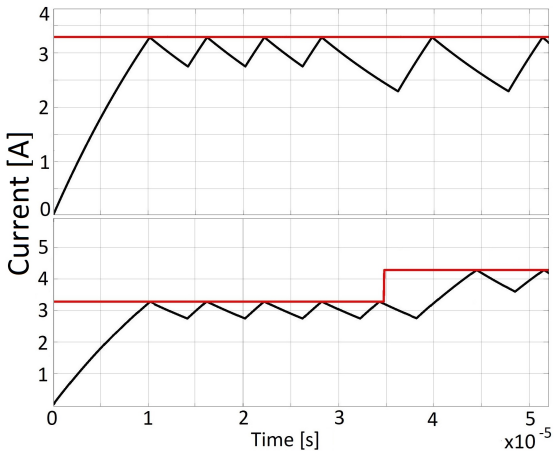

Fig. 9. T_{off} Perturbation (top); I_{max} Current perturbation (down)

Given the ripple from table I and T_{off} by (11), both the peak and the average current are fixed. Moreover, by using those parameters in (4), the inductance value is obtained:

$$L > \frac{V_{out} * T_{off}}{\Delta I_L} = 24\mu H \xrightarrow{+20\%} 30\mu H \qquad (12)$$

(considered 20% of inductance value uncertainty). Together with other non-idealities (on the R_{sense}, the N factor and the clock error) the total average current error will be about 2.9%.

The highest T_{on} is obtained for $V_{in,min}$:

$$\Delta I_L = \frac{7V - 3.5V}{30\mu H} \cdot T_{on,max} \rightarrow T_{on,max} = 5.1\mu s \qquad (13)$$

Therefore, the maximum switching period is $9.2\mu s$, i.e. a minimum switching frequency of $f_{sw,min} = 108kHz$.

Fig. 8 shows the load current when V_{in} increases from 4.5V to 27V. As a result, the rising slope increases in accordance with the (3). The switching frequencies are: 108kHz at 7V, 166kHz at 12V and 212kHz at 27V. The counter here operates with an internal oscillator of 10MHz.

Fig. 9 (top) shows the response to an abrupt positive perturbation on the T_{off} value. This reflects on the ripple and average values. Instead, Fig. 9 (down) shows an abrupt I_{max} reference change. The average current assumes a new value.

VI. Conclusions

The paper presents a PCMC Constant-T_{off} loop to precisely control the current features of a load in automotive application. The system is lighter and cheaper than most common PCMC solutions for two reasons: the use of a current sensing technique with an integrated low-side resistor to minimize the PCB usage space and the neglecting of the output filter C_{out}, avoiding moreover the presence of its ESL and repercussion on the Buck transfer function and bandwidth.

Transient simulations shown an excellent dynamic behaviour for input voltages between 4.5 and 27V, in agreement with the expected theoretical one. Even if the duty cycle may grow beyond 50%, no instability issues are encountered since the switching frequency is variable. No stabilization techniques are therefore needed. Even in worst cases, adding exaggerated and sudden perturbations on I_{max} and T_{off}, the system react fast and as predicted.

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