1MHz Gate Driver in Power Technology for Fast Switching Applications

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***Abstract*— The demand for low-cost integrated circuits for automotive applications is increasing, while their cost must remain low to maintain product competitiveness. In this scenario, to guarantee DC-DC Buck converters high-efficiency and low cost (in terms of external components) increasing switching frequency is mandatory. The main problems are inherent the parasitic inductances and the parasitic capacitance of power mosfet. This paper deals with the main critical aspects of increasing such switching frequency and show how to replace the external Schottky diode with an integrated structure. The case of a high-speed monolithic integrated circuit to control a load current is here proposed. Proper design allows to achieve switching frequency up to 1MHz with 94.4% efficiency.**

Keywords— gate driver, DC/DC converter, Buck,

I. INTRODUCTION

Day-by-day the demand for switching DC-DC converters is increasing over conventional converters because of their higher efficiency. Getting from the voltage battery to a few volts with power electronic circuits requires very large voltage conversion ratio. Primary converters, such as buck converters, use the large duty cycle to achieve large step-down ratios. The efficiency can be kept high by reducing losses, reducing the number of external components and reducing the dimensions of parasitic components (like Equivalent Series Resistor). Inductive DC-DC converters can accomplish this task but require large magnetic components (inductors), which cannot be integrated and, typically, feature low power efficiency at light or no load. This drawback can be mitigated by increasing the switching frequency from the typical ≈300kHz up to 1MHz and beyond, but this appears critical when high switching frequency has to be implemented in high-power nodes with very large devices and, then, very large parasitic capacitance to be driven. The trade-off between switching frequency and conversion efficiency will be part of the power transistor design. In [1] are presented the simulations results about the gate driver at 1MHz.

In many DC-DC converters applications [2]-[4] there is an external diode to charge the bootstrap capacitor and an external power transistor to supply the load. These external components increase the PCB size and cost and reduce efficiency due to the associated parasitic impedance. In this paper the on-chip implementation of such components is studied. The power transistor [5] and the block used to charge the bootstrap capacitor have been integrated on silicon, allowing minimizing capacities, inductances and resistances in the PCB. In this way it is possible increasing the gate driver frequency up 1MHz, with high dV/dt for V_{DS} on power transistor. The proposed gate driver, bootstrap circuit and level shifter are designed for a load that requires a constant current of 3A with an input voltage range of 4.5V to 27V.

The paper is organized as follows. The gate driver architecture and the block designs are presented in Section II. The experimental results are given in Section III, and Sections IV concludes the paper.

II. GATE DRIVER ARCHITECTURE AND BLOCK DESIGN

A. Gate driver Architecture

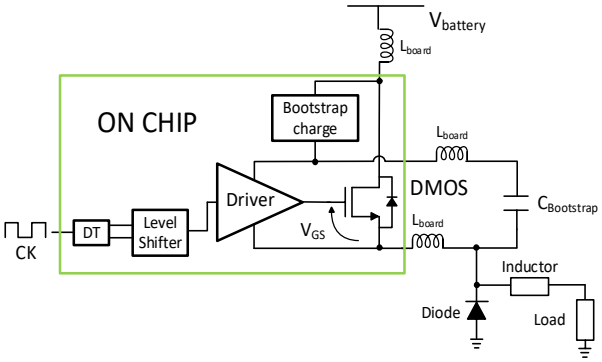

Fig. 1 Block diagram of gate driver

Fig. 1 shows the structure of the proposed on-chip HV gate driver in an asynchronous buck DC-DC converter. The main blocks are: the dead time generator, the level shifter, the inherent bootstrap charge, and the driver. $V_{bootstrap}$ is a floating voltage that can range from below ground to above battery voltage. In the next section, the operation of each block will be explained.

B. Dead Time Generator

The Dead Time Generator is the Timing Control (TC) block that provides an appropriate dead-time inserted between the switching on-phase and off-phase of the power transistor to avoid overlapping of the two states. The Dead Time Generator supports the level shifter to produce two signals:

one signal turns on the switch (ck_{low}) and the second one turns it off (ckq_{low}).

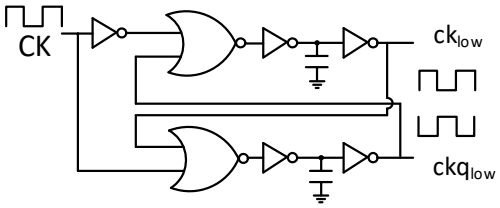

Fig. 2 Dead Time generator

The adopted 'analog' solution is shown Fig.2. The non-overlapping time is defined by means of two capacitors of the same value (2pF) to obtain ≈20ns non-overlapping time. To calculate the optimal dead-time in a given application, the fall time in the actual circuit needs to be taken into account. In addition, variations in temperature and device parameters could also affect the effective dead-time in the actual circuit. Therefore, the nominal 20ns dead-time is chosen to avoid any PVT variations to produce shoot-through current. This analog solution, for this technology, reduces the die area compared to the digital version.

C. Level shifter

A fast and robust level shifter is necessary to transfer the signals to switch on and switch off the high-side driver. The scheme of Fig. 3 is based on low and high voltage transistor. When the ck_{low} is high, the V_{ck_high} is a digital zero and vice versa when ck_{low} is low. The transistors M_1 and M_2 are high-voltage devices (HV), while other transistors are low-voltage devices, because the difference between $V_{bootstrap}$ and Vs (voltage source on power switch) will be properly limited by design.

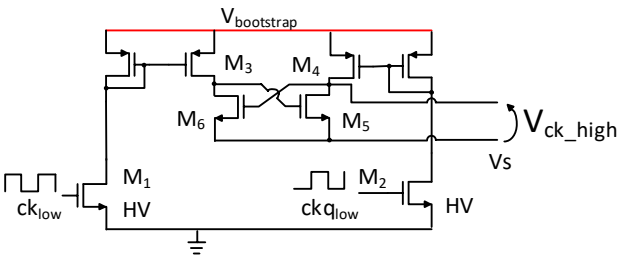

Fig. 3 Level Shifter

This level shifter operates with a floating supply voltage, indeed $V_{bootstrap}$ is above the battery voltage when the power transistor turns on. Two complementary clocks (ck_{low}, and ckq_{low}) generated by the Dead Time Generator drive this structure. Between the two signals, there is a dead time to stabilize the level shifter, preventing a non-switching due to excessively high frequency. When clock ck_{low} is high, M1 is turned on and M2 is off, in the first branch there is a current and, therefore, M3 turns on and the voltage on $V_{D(M3)}$ is:

$$V_{D(M3)} \approx V_{bootstrap} - V_{DS(M3)} \quad (1)$$

Therefore, transistor M5 turns on, because

$$V_{D(M3)} > V_{th(M5)} \quad (2)$$

while M6 turns off. The delay between input and output can be kept in order of 6.4ns enabling high speed operations. The transistors must be large enough to withstand voltage fluctuations without changing state. For this case, the current consumption is around 100uA.

D. Power switch

The power transistor design depends on the switching frequency and the associated losses. Fig. 4 shows the losses related to a power transistor with an $R_{ds(on)}$ equal to 150mOhm and that of a transistor with an $R_{ds(on)}$ equal to 50mOhm. As the switching frequency increases, the capacitive losses are more relevant than the conduction losses. On the other hand, for low frequency the power losses are proportional to the switch resistance. Therefore, a small power transistor 150mOhm is preferable when the frequency increases. As a consequence, also the occupied area reduces.

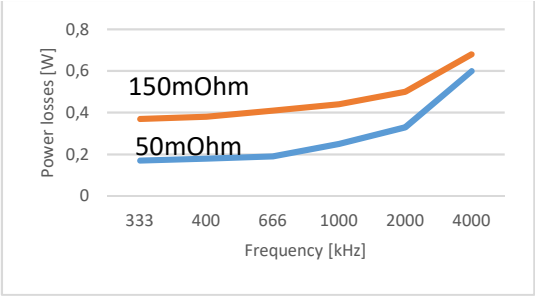

Fig. 4 Power losses on power switch vs frequency

E. Gate Driver

The gate driver in Fig. 5 determines the state of the power MOSFET. The gate driver is composed by a pair of low voltage MOSFET and it is designed to pilot a power transistor.

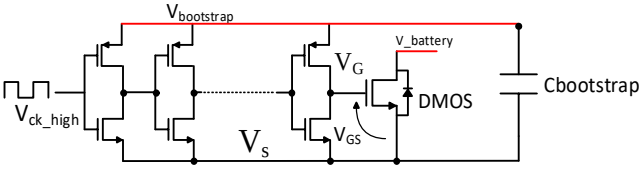

Fig. 5 Gate Driver

The delay between the input signals and the output signal for such a driver is negligible with respect to other delays.

Since NMOS offers higher mobility than PMOS, it is convenient to use the NMOS as high side power in terms of implementation area (while providing the same on-resistance during conductions). Because of the high frequency operation requirement, the higher ohmic power transistor of Fig. 4 has been selected. To design a fast switching on-chip gate driver, the equivalent gate capacitance of the power transistor has been calculated (C=1nF). From the basic equations below:

$$Q = C * \Delta V \quad (3)$$

$$Q = I * \Delta t \quad (4)$$

where Q is the equivalent charge, ΔV is the maximum V_{GS} on power transistor, Δt is the rise time of V_{DS} and I is the average gate current to charge the equivalent capacitor. Once the rising time is set, the above equations are exploited to obtain the average current to switch:

$$I = \frac{C*\Delta V}{\Delta t} = 300mA \quad (5)$$

Moreover, to design the gate driver last branch the following approximation is assumed:

$$\Delta t = 3 * \tau = R_{on_{pmos}} * C \qquad (6)$$

$$R_{on_{pmos}} < 10\Omega$$

To guarantee a secure margin, $R_{on_{pmos}}$ is designed to be 2Ω. Moreover, during simulations W/L=48 with multiplicity equal to 100 has been used (Fig. 5) and for the $R_{on_{nmos}}$ the ratio is 2.5 times smaller.

F. Bootstrapping technique for N-type high-side switch

This circuit recharges the external bootstrap capacitor, used to generate the voltage for turning on the power switch. This system is preferred to the charge pump since it is faster and this is mandatory for the target high switching frequency.

The bootstrapping scheme is illustrated in Fig. 6. During the switching operations, when the power switch is off, the electric charge is stored in the capacitor from $V_{battery}$, resulting in the voltage across of the capacitor to be $V_{bootstrap} = I_{dc}*R_{ref}$. The switch M2 inside the level shifter (Fig. 3) turns off, while M1 must be turned on, and the voltage across the bootstrap capacitor acts as a temporary supply voltage for the level-shifter and as a buffer for power transistor. As soon as the power transistor is switched on, its source voltage is pulled up as well as the auxiliary supply voltage level $V_{bootstrap}$ because of the bootstrap capacitor. Note that the parasitic diode of the HV NMOS becomes reversely biased since the bulk terminal is always biased such that its voltage is below the input one. Afterwards, the bootstrap capacitor slowly discharges through the level-shifter and the buffers. However, its capacitance is large enough to maintain a sufficient charge until the switch turns off again. Furthermore, Fig. 3 shows that the V_{ck_high} may exceed of few volts the battery voltage, which is approximately the value reached by the out_1 node minus the voltage drop on power transistor. This scheme allows to charge the bootstrap capacitor with switching frequencies >1MHz, because the capacitor starts to charge when the voltage bootstrap is one Vth_{MHV} lower than the voltage battery.

To charge the bootstrap the current coming from a bandgap reference is used. This bandgap current makes the bootstrap voltage insensitive to temperature variation. Due to the M_{HV} body effect, its threshold increases leading to $V_{bootstrap}$ inaccuracy (the reference voltage will be the sum of $V_{bootstrap}$ and Vth_{MHV}). To have the same voltage between the $V_{bootstrap}$ and the node above R_{ref}, a diode-connected transistor it is used to compensate the V_{GS} drop over M_{HV}. The proper bootstrap capacitance is selected according to the application as:

$$C_{bootstrap} \geq \frac{Q_{tot}}{\Delta V_{bootstrap}} = \frac{3nC}{0.4V} = 7.5nF \qquad (7)$$

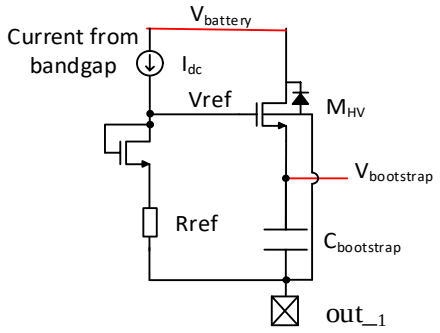

Fig. 6 Bootstrap circuit

III. Experimental Results

The proposed device has been realized in a low-cost BCD technology. Fig. 7 and Fig. 8 shows the measured falling time (6.35V/ns) and rising time (3.55V/ns) behavior. In reference [6] for this time was 5ns for rise time e 10ns for fall time.

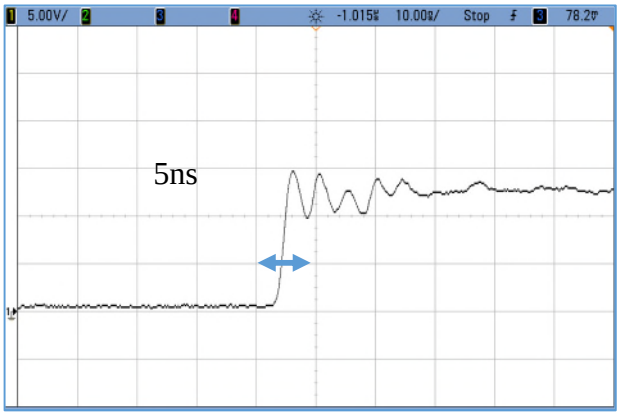

Fig. 7 VDS rise time Vin = 12V

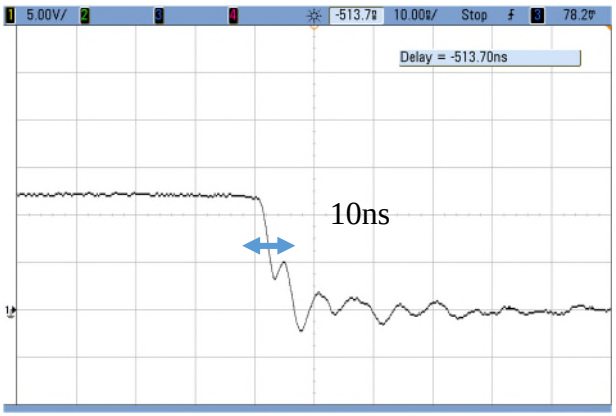

Fig. 8 V_{DS} fall time V_{in} = 12V

The circuit has been tested with three load (5, 10, 50Ω), at 12V of input voltage. The ringing are mainly caused by the parasitic inductances present in the bonding wires.

The chip has been tested at the edges of the possible duty cycle values, i.e. for the minimum duty cycle below 5% (see Fig. 9) and the maximum duty cycle above 90% (see Fig.10). This structure allows to reach a very low and high duty cycle up to 1MHz (Fig. 11), as a consequence the input voltage can take values very close to the Vout or over 27V, and inductor can be reduces up to 36% (from 47uH to 30uH).

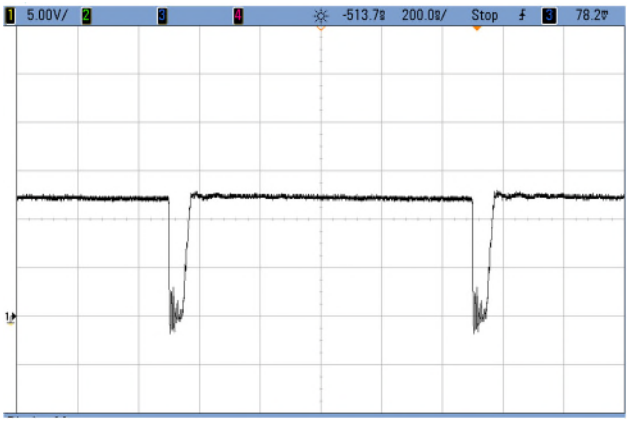

Fig. 9 Duty Cycle 5%

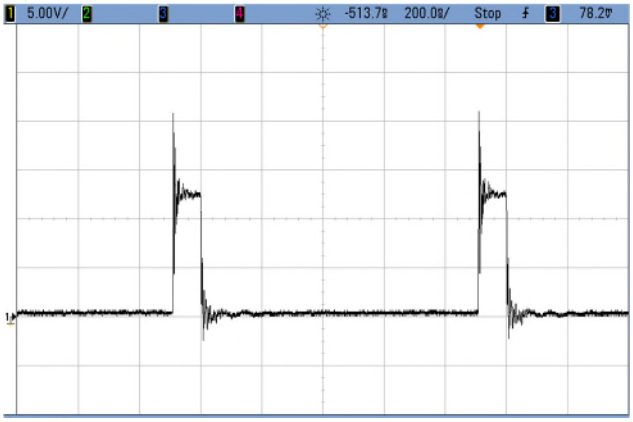

Fig. 10 Duty Cycle 90%

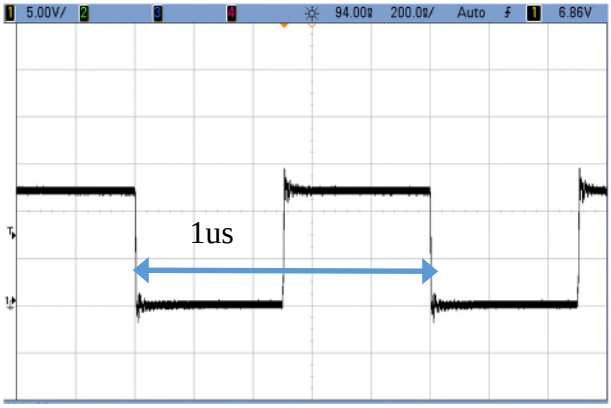

Fig. 11 V_{DS} on power switch

A. *Efficiency*

Tab. I presents results about the efficiency for standard conditions. To verify the efficiency, duty cycle values of 30% and 50% has been used. This configuration allows to check that at the same load and the same input voltage, the case with a duty cycle of 30% will be worse than that with D = 50%. Because with 30% of duty cycle, the Schottky diode leads for 70% of the time and this reduces the overall efficiency. Tab. II presents the efficiency of this work compared to the other literature DC-DC.

TABLE I. EFFICIENCY

Efficiency			
Vin [V]	***Duty Cycle [%]***	***Load [Ω]***	***η [%]***
12	50	50	90,04
12	50	10	92,28
12	50	5	89,01
12	30	50	88,54
12	30	10	92,00
12	30	5	90,45

IV. CONCLUSIONS

In this paper an on-chip gate driver has been presented. The implemented high speed design solutions allow rapid state transitions of the high-side switch with an efficiency of 92.28%. An additional advantage is in the usage of a low-cost BCD technology in the design. As consequence of that, the circuit reaches high efficiency even in a high frequency regime without giving up on a competitive cost for the final product.

TABLE II. PERFORMANCE COMPARISONS OF DIFFERENT BUCK CONVERTERS

	Comparison			
	LTC3630 [6]	***LM5007 [7]***	***LM5017 [8]***	***This Work***
Converter topology	Synch. Buck	Async. Buck	Sync. Buck	Asynch. Buck
Input Voltage (V)	12.5 - 76	12 - 75	12.5 - 95	4.5 - 27
Fsw (kHz)	N. A.	400	200	1000
Output voltage (V)	12	10	10	6
Max Output Current (A)	0.5	0.4	0.6	3.5
Efficiency	92% at Vin = 24V	93.7% at Vin = 15V	92.5% at Vin = 24V	92.28% at Vin = 12V

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REFERENCES

[1] Di Lorenzo R., Gasparri O., Pidutti A, Del Croce Paolo, Baschirotto A., On-Chip Power Stage and Gate Driver for Fast Switching Applications, In *2019 26th International Conference on Electronics Circuits ans Systems (ICECS)*. IEEE.

[2] Bau, P., Cousineau, M., Cougo, B., Richardeau, F., Colin, D., & Rouger, N. (2018, July). A CMOS gate driver with ultra-fast dV/dt embedded control dedicated to optimum EMI and turn-on losses management for GaN power transistors. In *2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)* (pp. 105-108). IEEE.

[3] Subotskaya, V., Mihal, V., Tulupov, M., & Deutschmann, B. (2018). Optimized gate driver for high-frequency buck converter. *e & i Elektrotechnik und Informationstechnik*, *135*(1), 40-47..

[4] Mednik, A. (2005). Automotive LED lighting needs special drivers. *Power Electronics Technology Magazine.*

[5] Elmoznine, Abdellatif, Buxo, Jean, Bafleur, Marise, & Rossel, Pierre (1990). The smart power high-side switch: description of a specific technology, its basic devices, and monitoring circuitries. *IEEE Transactions on Electron Devices*, *37*(4), 1154-1161.

[6] Liu, Z., Cong, L., & Lee, H. (2015). Design of on-chip gate drivers with power-efficient high-speed level shifting and dynamic timing control for high-voltage synchronous switching power converters. *IEEE Journal of Solid-State Circuits*, *50*(6), 1463-1477.

[7] Texas Instruments Inc., LM5007 Datasheet: High Voltage (80 V) Step Down Switching Regulator, Mar. 2013.

[8] Texas Instruments Inc., LM5017 Datasheet: 100 V, 600 mA Constant On-Time Synchronous Buck Regulator, Dec. 2013.