D7.6

Yield estimation and prediction figures of merit and yield detracting factors determination

Project title:	iDev40: Integrated Development 4.0
Project start date:	1st of May 2018
Duration:	36 months

Deliverable type:	Report
Activity and Work package contributing to the deliverable:	Task 7.2.2 / WP 7
Due date:	31.07.2020
Actual submission date:	30.07.2020

Responsible lead organization:	Technical University Cluj-Napoca (UTC)
Lead Author:	Marina Țopa (UTC)
Dissemination level:	Public
Reviewer:	Cristian Boianceanu / Infineon Technologies Romania CO&SCS (IFRO)
Revision Date:	27.07.2020
Document Reference	D81

This project has received funding from the ECSEL Joint Undertaking under grant agreement No 783163. The JU receives support from the European Union's Horizon 2020 research and innovation programme. It is co-funded by the consortium members, grants from Austria, Germany, Belgium, Italy, Spain and Romania.

Authors (all contributors to the Deliverable)

	Name	Chapters
Technical University Cluj-Napoca	Ingrid Kovacs	2, 3
	Marina Țopa	1, 2.1, 3.2
Infineon Technologies Romania	Emilian David	2, 3

Publishable Executive Summary

This deliverable focuses on activity performed in **tasks 7.2.2** (Design Methodology for Reliability Analysis and Yield Prediction) in the direction of yield prediction. This activity is related to **Use Case 4** (Yield Prediction with Knowledge-Based Modelling).

The deliverable is structured into 3 chapters:

- A general introduction presented the scope of the work and the partners involved
- Chapter 2 presents the proposed methodologies for yield analysis for both univariate and multivariate cases. Comparisons with other approaches presented in the literature and figures of merit are also presented. For both cases, the comparison was performed on integrated circuit (IC) verification data provided by IFX. The results showed that the *FP* (Failure Probability) metric based on statistical distribution modelling is the most suitable for IC yield estimation (univariate), as it has the lowest variance in estimation. For the case of multivariate yield estimation and prediction, the proposed *DIMYE* (distribution-model based multivariate yield estimation) metric was applied for the yield prediction of an IC product and proved its advantages over other multivariate yield estimation metrics.
- Chapter 3 presents a yield detractors analysis method based on the correlations between the electrical parameters and the technology parameters. This correlation information can be used not only to identify the yield detractors, but also anticipate eventual redesign of an IC product already at simulation. The methodology was validated on IC verification data provided by IFX.

Activity in task 7.2.2 has started on November 26th, 2019 due to delays in the release of funds by the Romanian funding authority.

Key Words

manufacturing yield assessment, yield prediction, yield detractors detection, root cause discovery of yield loss, pre-silicon verification, post silicon verification, distribution modelling.

Contents

Publishable Executive Summary ..... **III**

1 Introduction **1**

2 Design methodology for yield analysis **3**

2.1 Introduction to yield estimation and its figures of merit 3

2.2 Methods for univariate yield estimation and figures of merit 3

2.3 Methods for multivariate yield estimation and figures of merit 14

2.4 Conclusions 20

3 Method for yield detracting factors' determination **22**

3.1 Overview 22

3.2 Method of yield detractors' detection based on process parameters 22

3.3 Conclusions 29

4 List of Abbreviations **30**

5 References **31**

List of Figures

Figure 2.2.1 The relationship between the actual and allowable process spread 5

Figure 2.2.2: Yield estimation in terms of the probability distribution function 7

Figure 2.2.3: Yield estimation in terms of the cumulative distribution function 7

Figure 2.2.4: Distribution models characterizing semiconductor data 8

Figure 2.2.5: The proposed distribution fitting flow (Kovacs et al. 2017) 8

Figure 2.2.6: The distribution statistics of the data set from IC verification 9

Figure 2.2.7: Examples of empirical and theoretical (using *distFit*) *cdfs* of several parametric distributions of the inspected data set 10

Figure 2.2.8 The standard deviation of the $\boldsymbol{FP}$ using the *distFit*, OOS and equivalent $\boldsymbol{FP}$ of the $\boldsymbol{Cpk}$ metrics for one EP with lognormal distribution 11

Figure 2.2.9 The standard deviation of the $\boldsymbol{FP}$ using the *distFit*, OOS and equivalent $\boldsymbol{FP}$ of the $\boldsymbol{Cpk}$ metrics for one EP with normal distribution 11

Figure 2.2.10: The standard deviation of the $\boldsymbol{FP}$ using the *distFit*, OOS and C_{pk} metrics on several EPs 12

Figure 2.2.11: The standard deviation of the $\boldsymbol{FP}$ using the *distFit* and OOS metrics on several EPs 12

Figure 2.2.12: The statistics of discrepancies between quantile $\boldsymbol{Cpk}$, OOS and *distFit* 13

Figure 2.2.13: The distribution statistics of the EPs 13

Figure 2.3.1: Illustration of the core idea of the proposed *DIMYE* method 16

Figure 2.3.2: The steps of the proposed *DIMYE* method 16

Figure 2.3.3: Illustrating step 2 of the proposed method 16

Figure 2.3.4: Illustrating step 5 of the proposed method 17

Figure 2.3.5: The distribution statistics of the EPs 17

Figure 2.3.6: Example 1 of cluster of correlated EPs 18

Figure 2.3.7: Example 2 of cluster of correlated EPs 18

Figure 2.3.8: The variance of estimation of the OOS counts method and the OOS using the DIMYE method 19

Figure 2.3.9: The *cdf* of the original and transformed data (lognormal distribution) 19

Figure 2.3.10: The *cdf* of the original and transformed data (Gamma distribution) 20

Figure 3.2.1: Illustration of the IC verification phases and causes of yield loss at DoE testing 23

Figure 3.2.2 The yield detractors' detection analysis flow 24

Figure 3.2.3: The *cdfs* of EP_1 in simulation and DoE testing 24

Figure 3.2.4: The box plots of EP_1 in DoE testing 24

Figure 3.2.5: The *cdfs* of EP_3 in simulation and DoE testing 25

Figure 3.2.6: The *cdfs* of PCM_1 in simulation vs. DoE testing vs. history 26

Figure 3.2.7 The *cdfs* of PCM_2 in simulation vs. DoE testing vs. history 26

Figure 3.2.8: The box plots of PCM_1 in DoE testing 27

Figure 3.2.9: The box plots of PCM_2 in DoE testing 27

Figure 3.2.10: Illustrating the first order effect of PCM_2 on EP_1 28

Figure 3.2.11: Illustrating the first order effect of. PCM_2 on EP_1 (wafers with yield loss highlighted) 28

Figure 3.2.12: Illustrating the quadratic effect of PCM_2 on EP_1 28
Figure 3.2.13: Illustrating the quadratic effect of PCM_2 on EP_1 (wafers with yield loss highlighted)..... 29

List of Tables

Table 2.2.1: Various $\boldsymbol{Cpk}$ values and the corresponding process yield (Nist n.d.) 5

Table 2.3.1 The multivariate yield estimation using the *simple count* method 14

Table 2.3.2: Yield loss estimation using different yield loss prediction methods (wafer 1) 19

Table 3.2.1: Top weighted correlation scores of PCMs vs EP_1 25

1 Introduction

This deliverable focuses on activity performed in **tasks 7.2.2** (Design Methodology for Reliability Analysis and Yield Prediction) in the direction of yield prediction. This activity is related to **Use Case 4** (Yield Prediction with Knowledge-Based Modelling).

The work focuses on the development of accurate metrics and figures of merit for the IC yield estimation and prediction. The goal is to develop metrics for both univariate (per parameter) and multivariate (per product) yield estimation which overcome the limitations of current metrics: normality assumption and high variance of the estimation. The metric s which are developed are based on a proof of concept work done by UTCN in partnership with IFRO. The validation of the methods is done on IC verification data provided by IFX.

The goal of the task 7.2.2 is to simplify the analysis by introducing unique metrics for the multivariate yield. For this new methods for yield assessment, prediction and optimization will be developed, methods that are based on combining production monitoring data and IC test data gathered on a small sample size to predict the yield for a given product or in the decision making process during the development of the product (yield prediction based design decisions) and the production, e.g. if there are violation of process or machine parameters).

One objective is related to product development methodologies for enhanced manufacturing yield assessment, prediction and optimization based on multivariate distribution modelling. In Use Case 4 these methodologies will be employed for different design to check their prediction capabilities and target possible yield improvement based on design optimization. The current methods for yield prediction try to simplify the analysis by introducing unique metrics for the multivariate yield. We extended the distribution modelling together with other statistical approaches to estimate the yield taking into account also the correlations between test and process monitoring parameters. Using this approach, we derive figures of merit for assessing the yield prediction confidence level. A second goal is to propose figures of merit for the yield estimation/prediction confidence level and the identification of yield loss factors.

The team from Infineon Technologies Romania (IFRO) participating in this activity is part of the technology platform development department - IFRO DCBUC ATV PTP - for integrated circuits for automotive applications. These team is specialized in the development of methodologies, platforms and analysis and verification models that aim to: determine and improve the reliability of integrated power circuits, determine and improve production efficiency and quality assurance verification process both in the pre-production as well as post-production phase.

The team from Technical University Cluj-Napoca (UTCN) is part of the Electronics, Telecommunications and Information Technology Faculty. Its task in the project is the development of advanced methods of manufacturing yield assessment, yield prediction, yield detractors detection and root cause discovery.

Within **task 7.2.2** IFRO collaborated with UTCN in the study of accurate yield estimation and prediction figures of merit and yield detracting factors' determination. UTCN together with IFRO define multi-variable analysis methods that can use the data and the existing infrastructure within the company and finally allow the prediction of the yield. UTCN performs the implementation and evaluation of these methods on test data sets and together with IFRO the evaluation in the industrial environment provided by IFX. Both teams then assess the accuracy of yield estimation and define figures of merit.

The project was funded from European Structural and Investment Funds (ESIF). Activity in task 7.2.2 has started on November 26th, 2019 due to delays in the release of funds by the Romanian funding authority and accumulated a duration of 6 months, so far.

After this introduction, the deliverable is structured in 3 parts. Chapter 2 starts with a presentation of the design methodology for the yield analysis. It describes methods and metrics used for the univariate

yield and also multivariate yield estimation. Special focus will be set to the Failure Probability (*FP*) using distribution models, which is applicable for univariate yield estimation. Validation and comparison of the *FP* metric to two other metrics is also included. The results are obtained on IC verification data provided by IFX. In this chapter, a multivariate yield estimation metric is also proposed. Again, it is compared to other multivariate yield estimation metrics based on IC verification data.

Chapter 3 focuses on methods for yield detracting factors' determination. The core of the proposed method relies on the simple, yet efficient correlation information of process and electrical parameters. Results are shown for the yield loss inspection of an IC product.

At the end of the each section, a set of unified conclusions is presented.

2 Design methodology for yield analysis

2.1 Introduction to yield estimation and its figures of merit

Semiconductor integrated circuits (ICs) are part of many applications in nowadays life. They are integral part of laptops, mobile phones, consumer (household) electronics and cars. To guarantee that they fulfill the highest quality standards, especially in automotive applications, these IC chips have to be tested and verified thoroughly. The percentage of IC chips that meet specifications is given by the yield. More explicitly, the yield characterizes the production efficiency, i.e. the number of good chips in a production batch that can be delivered to the customers.

Ensuring a good yield for today's ICs is more important than ever due to the ever-increasing production costs of modern nanometer technologies, the very expensive testing required by more complex circuits and systems, and the increasingly stringent regulations on safety and robustness. Moreover, the inherent variation of the process affects the quality of the IC, causing yield losses. Therefore, methods are needed for a correct and accurate approach to IC yield analysis and the discovery of the cause that decreases yield in a short time. Mass production of semiconductor ICs by using photolithography techniques can produce millions of ideally identical copies of a prototype. However, variations inherent to any manufacturing process result in non-identical ICs, even within the same production batch. Thus, the importance of ensuring a good yield for these ICs is more important than ever. This evolvement has raised new challenges for IC qualification:

1. Complex products come with a big number of parameters to be tested (hundreds), which significantly complicates the yield analysis. On the other hand, the wafers specifically processed to obtain information about the process corners represent only a snapshot of the process variation, therefore methods are needed that can extract the maximum information from the available results.

2. The yield analysis should not only assess if the current design will have a high manufacturing yield, but should also identify yield detractors and quantify the impact they have on the yield, so that the optimization of it may be possible at the next development iterations.

The standard yield prediction methods currently used simplify the analysis by introducing unique values (metrics, figures of merit) for the yield. The main limitation of these methods is that they assume that the individual distributions of the electrical parameters are Gaussian, which is not the case in most cases. Only a few studies consider the non-normal distributions of the parameters.

Next, several univariate yield estimation metrics will be described briefly in Section 2.2, emphasizing both advantages and limitations. Among all, the *FP* metric based on the distribution modelling gives the most intuitive measure of the yield. Also, it is applicable on non-normally distributed data. Moreover, it proved to have lower variance in estimation than other common yield estimation metrics. The comparison was performed on IC verification data provided by IFX.

Section 2.3 describes multivariate yield estimation approaches and metrics. Again, comparison of the proposed metric and current metrics was performed. The dataset for validation was provided by IFX.

2.2 Methods for univariate yield estimation and figures of merit

The yield has a very specific meaning for circuit design and verification (McConaghy et al. 2013). In circuit design, yield is measured at several points of the design and manufacturing flow. The yield estimated during circuit simulation is called parametric yield (McConaghy et al. 2013). In a similar way, the manufacturing yield is calculated from the actual number of chips that meet specifications. In the ideal case, the parametric yield and the manufacturing yield return identical values, but due to several sources of variations (wafer-to-wafer and die-to-die, within die) the two values are different. However, improvement of the parametric yield usually lead to improvements of the manufacturing yield. Next, several yield estimation methods will be described. Most of these methods have been implemented and included in the M7.1 Milestone report *"Software package for product level yield estimation"*

- **Simple count method used for yield estimation**

For yield estimation of non-normal data, one simple metric is the failure count, i.e. counting the chips falling outside the specification limits, also called out-of-spec (OOS) count:

$$OOS = \frac{\#chips\ out\ of\ spec}{total\ \#chips} \tag{1}$$

Note that this method has no statistical assumptions and has the disadvantage of high variance in estimation, especially for low sample sizes.

Confidence intervals of the simple count method

The simple count method can be seen as an experiment with two outcomes, labeled as failure (chip does not meet specification) and success (chip meets specification). Then, the experiment can be seen as a binomial experiment. The literature provides several methods for the confidence interval estimation of the binomial proportion (Brown et al. 2001), like the Agresti-Coull method (Agresti and Coull 1998) and the Wilson method (Wilson 1927). The Wilson CI estimation is detailed below:

$$upper\ limit = \frac{\widehat{yield} + \frac{z_{1-\alpha/2}^2}{2N} + z_{1-\alpha/2}\sqrt{\frac{\widehat{yield}(1-\widehat{yield})}{N} + \frac{z_{1-\alpha/2}^2}{4N^2}}}{1 + \frac{z_{1-\alpha/2}^2}{N}} \tag{2a}$$

$$lower\ limit = \frac{\widehat{yield} + \frac{z_{\alpha/2}^2}{2N} + z_{\alpha/2}\sqrt{\frac{\widehat{yield}(1-\widehat{yield})}{N} + \frac{z_{\alpha/2}^2}{4N^2}}}{1 + \frac{z_{\alpha/2}^2}{N}} \tag{2b}$$

where z denotes the percent point function of the standard normal distribution and N is the sample size. This interval has good properties even for a small number of trials and/or an extreme probability.

- **Process capability indices used for yield estimation**

In order to characterize the process with respect to specification compliance of the process parameters, one usually compares the natural variability of the process with the process specification limits. For this purpose, a set of methods of process capability indices (PCIs) have been reported in literature; to mention only a few: C_p, C_{pk} and S_{pk} (Pearn et al. 1998; Kotz and Johnson 1992; Chen et al. 2003). Figure 2.2.1 describes the relationship of the allowable and actual process spread.

The PCIs have been adopted also for yield estimation. In this sense, the objective is not to test the specification compliance of the process, but rather to test the specification compliance of the electrical parameters which are affected by process variation.

The main advantage of the process capability indices is that they are easy to understand and straightforward to apply. However, their main limitation is that they assume a normal distribution of the parameters, which is often not held in IC yield and characterization analysis.

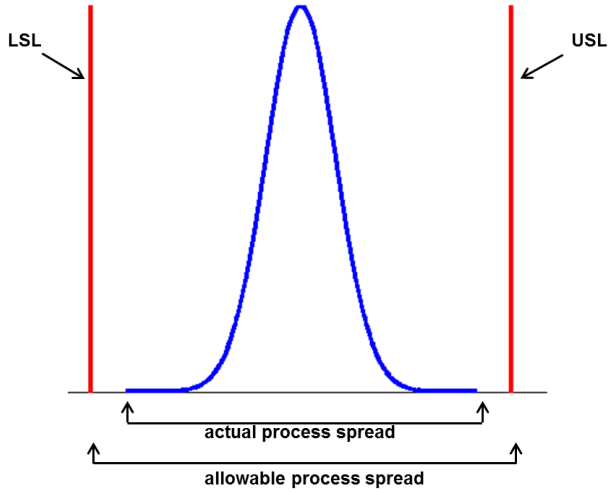

Figure 2.2.1 The relationship between the actual and allowable process spread

- The C_{pk} metric

The C_{pk} is a metric largely used in industry that estimates the capability of a normal distribution [AEC], (Pearn et al. 1998; Kotz and Johnson 1992; Kotz and Johnson 2002) and is computed as described in the equation below. It takes into account the magnitude of process variation as well as the degree of process centring, which measures process performance based on yield (proportion of conformities).

$$C_{pk} = min\left\{\frac{USL-\mu}{3\sigma}; \frac{\mu-LSL}{3\sigma}\right\} \quad (3)$$

where μ and σ are the mean and the standard deviation of the process, respectively.

Table 2.2.1 describes the process yield for commonly used C_{pk} values, along with the corresponding sigma level and the process fallout in terms of ppm (parts-per-million) (Nist n.d.). In the optimal case, the C_{pk} has a value at least equal with 2 to ensure 6 sigma capability.

Table 2.2.1: Various C_{pk} values and the corresponding process yield (Nist n.d.)

C_{pk}	Sigma level (σ)	Process yield	Process fallout (in terms of ppm)
0.33	1	68.27%	317311
0.67	2	95.45%	45500
1.00	3	99.73%	2700
1.33	4	99.99%	63
1.67	5	99.9999%	1
2.00	6	99.9999998%	0.002

Confidence intervals (CIs) of the C_{pk}

Assuming normally distributed data, confidence intervals for sample $\hat{C}_{pk}$ have been derived (Zhang et al. 1990). Note that the estimate of C_{pk}, $\hat{C}_{pk}$, is obtained by replacing μ and σ by $\bar{x}$ and s, respectively. The following approximation is commonly used in practice:

$$C_{pk} = \hat{C}_{pk} \pm z_{1-\alpha/2}\sqrt{\frac{1}{9N} + \frac{\hat{C}_{pk}^{\ 2}}{2(N-1)}} \quad (4)$$

where z denotes the percent point function of the standard normal distribution, N is the sample size and α is the confidence level. An important note is that the sample size should be at least 25 before these approximations are valid. In general, however, N≥100 samples are needed for capability studies.

- The quantile C_{pk} metric

Clements (1989) proposed the quantile C_{pk} index that accounts for the insensitivity to the shape of the distributions and is described as:

$$C_{pk} = min\left\{\frac{USL - m}{q_{0.99865} - m}; \frac{m - LSL}{m - q_{0.00135}}\right\} \quad (5)$$

where m denotes the median of the data and $q_{0.99865}$, $q_{0.00135}$ are the percentiles corresponding to probabilities 0.99865 and 0.00135, respectively. These percentiles correspond to the 3 sigma spread of a normal distribution.

Note that this metric presents a high variance in estimation for low sample sizes. For example, for the estimation of the percentiles, one needs 10000 samples for a solid $q_{0.00135}$.

Confidence intervals (CIs) of the quantile C_{pk}

There is no direct formula for the confidence limit estimation of the quantile C_{pk} metric. A solution to compute the CIs is to apply the bootstrapping method, which allows the estimation of the sampling distribution of almost any statistic using random sampling methods.

- **Density-based yield estimation**

Figure 2.2.2 illustrates the yield in terms of distributions. Note that the yield is the area under the *pdf* where it meets the target specifications, LSL (lower specification limit) and USL (upper specification limit) .This may be simply mapped to the *cdf* as illustrated in Figure 2.2.3.

Then, the failure probability (FP), i.e. the probability that x falls outside the specification limits is calculated as:

$$FP = 1 - P(LSL \leq x \leq USL) = 1 - \left(F_x(USL) - F_x(LSL)\right) \quad (6)$$

where $P(LSL \leq x \leq USL)$ represents the probability of x lying in the interval $[LSL;\ USL]$.

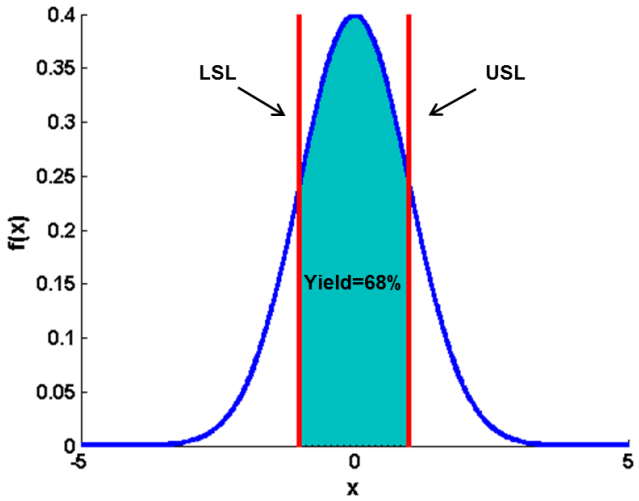

Figure 2.2.2: Yield estimation in terms of the probability distribution function

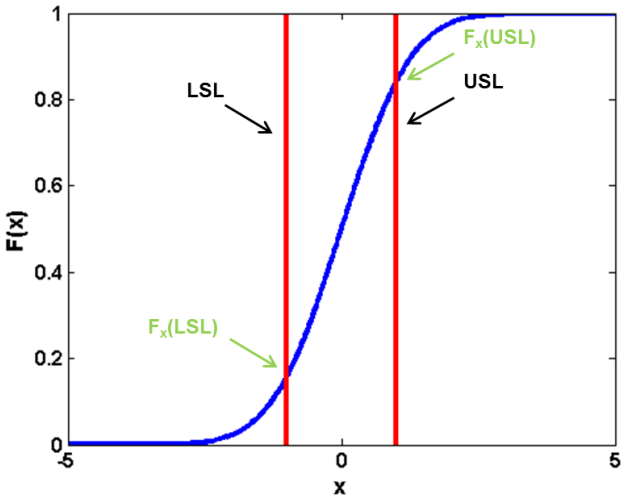

Figure 2.2.3: Yield estimation in terms of the cumulative distribution function

The FP can be directly mapped to the yield loss. One only has to know the distribution of the data; then, the *cdf* estimation is straightforward.

Confidence intervals (CIs) of the *FP*

As the population data is usually not available in IC verification, the distribution parameters are only estimates of the true parameters. Estimates usually desire CIs and these give an indication of how much uncertainty there is in the estimate at a specific confidence level.

As the FP is also an estimate and implies the *cdf*, which in turn depends on the distribution parameter estimates, it is desired to compute a confidence interval also for this metric. The confidence interval of the *FP* using distribution models can be deduced using the confidence limits of the distribution parameters.

The proposed distribution fitting (*distFit*) approach used for Failure Probability (*FP*) estimation of ICs

The literature provides a large number of distributions for statistical applications. The figure below presents a summary of the shapes of several distributions characterizing semiconductor data. Note that for other parameter settings, the distributions can take various different shapes.

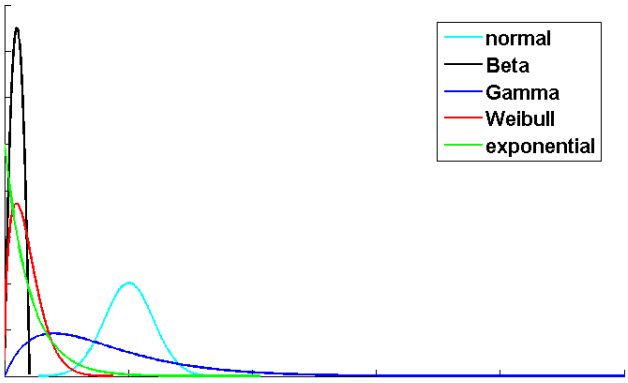

Figure 2.2.4: Distribution models characterizing semiconductor data

The proposed distribution fitting (*distFit*) flow (Kovacs et al. 2017) is presented in Figure 2.2.5. It includes a series of goodness-of-fit hypothesis tests where the assumption of the data to come from a specified distribution type is tested. A predefined flow of distributions to fit is specified a-priori and the algorithm quits as soon as the first distribution fit is accomplished, i.e. the hypothesis of the data to come from the tested distribution is not rejected. A number of eight parametric distributions like the normal, Box-Cox transformation to normal, Beta, Gamma, extreme value, exponential, lognormal and Weibull are included in the flow, along with the kernel distribution estimation for the nonparametric distribution estimation cases. The shapes of the above mentioned distributions cover most of the real data distributions of semiconductor production processes.

Note that the general assumption about the data is that it has normal distribution; this is the reason why the first step of the *distFit* is the normal fit test. However, this is not always true, so also other distributions have to be included in the flow in order to obtain accurate distribution models.

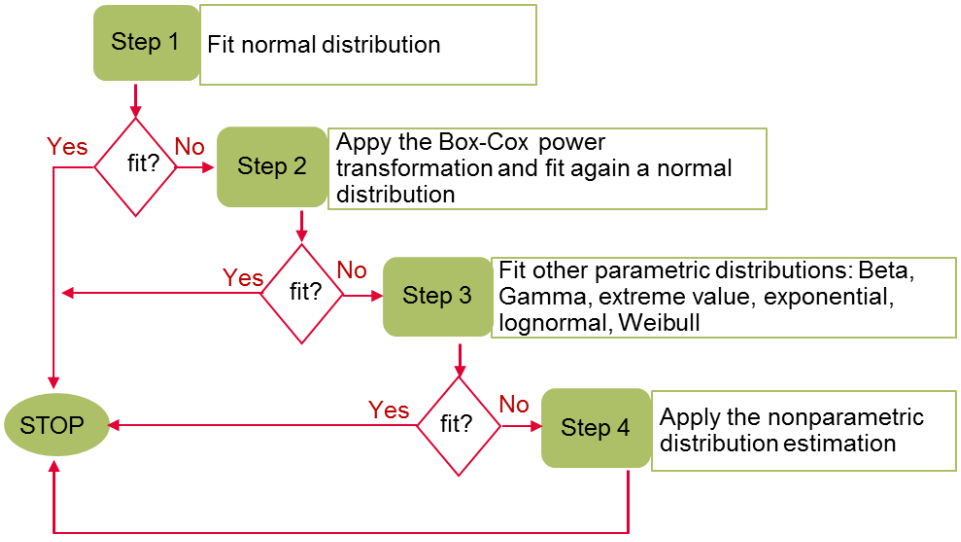

Figure 2.2.5: The proposed distribution fitting flow (Kovacs et al. 2017)

The second step of the *distFit* flow is the Box-Cox transformation (Box and Cox 1964) which attempts to transform non-normal data to normally distributed data. However, this is not a guarantee for normal distribution, so if the Anderson-Darling goodness-of-fit test is rejected, other parametric distributions are fitted to the data. The next options of distribution fitting are the Beta and Gamma distributions, because these cover various distribution shapes, followed by other parametric options such as extreme value, exponential, lognormal and Weibull parametric distributions. If none is fit to the data, the kernel density estimation is applied, which is a nonparametric distribution estimation method.

Figure 2.2.6 illustrates the distribution statistics of a data set representative for IFX product(s) from IC verification phase. Indeed, only about 30% of the data is normally distributed and the Box-Cox

transformation succeeds to transform only an additional 10% of the data to normal. Therefore, other distributions also have an important contribution to fitting accurate distribution models.

Figure 2.2.7 illustrates several examples of *cdfs* of parametric distributions. The empirical *cdf* is built using the information from the samples (by assigning equal probability to each observation in a sample), while the theoretical cdf is built using the *distFit* approach. Note that these examples are real examples from the data set from Figure 2.2.6.

Distributions, especially parametric ones, offer more solid statistics compared to individual data samples' handling. They are a compact way of representing the characteristics of a data using statistical information.

Moreover, distribution models can be used for performance assessment of ICs. Once the distribution of the data is known and the specification limits are defined, the failure probability calculation, i.e. the yield loss, is straightforward. As a long-term target, distribution models can be used as inputs to simulations.

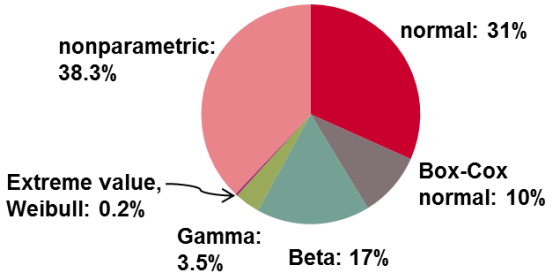

Figure 2.2.6: The distribution statistics of the data set from IC verification

Next, some validations of the *FP* metric will be done, along with comparison to the performance of other yield estimation methods. In order to validate the accuracy of the FP estimation using the *distFit* method, real production data was used, which included several distribution types and a high number of measured chips (>10000). The accuracy of the FP estimate using *distFit* was compared to two metrics highly used in verification processes: the *OOS* counts (simple count method) and quantile C_{pk} .

Before giving the overall results about the validation of the *distFit* method, some examples are given. A first approach for validation of the accuracy of the FP metric was to consider only a sample of the measured data for a single EP (electrical parameter) with a non-normal distribution (namely lognormal distribution), ranging from 100 to 10000 samples.

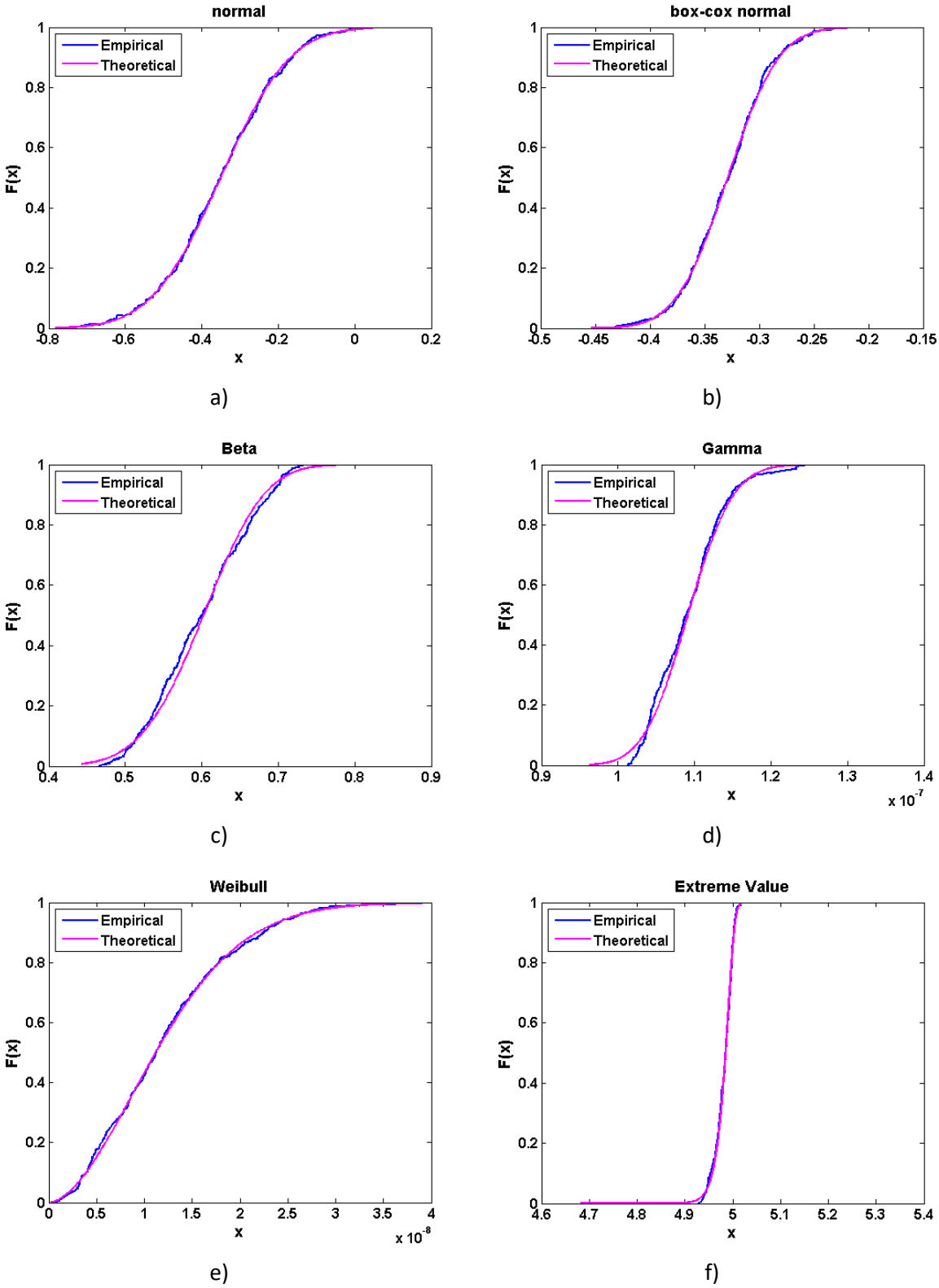

Figure 2.2.7: Examples of empirical and theoretical (using *distFit*) *cdfs* of several parametric distributions of the inspected data set

Note that the FP of this EP considering all measured chips was $FP = 2.997 \cdot 10^{-4}$. For each selected sample size, $\#Samples$, 1000 subsets were randomly selected and the FP using *distFit*, the OOS and the equivalent FP of the quantile C_{pk} were computed in each of the 1000 subsets. Then, the standard

deviation (*std*) of each metric was computed in each of the 1000 subsets with the sample size *#Samples*. Figure 2.2.8 illustrates the results.

It can be noticed that the *distFit* obtains lower variance in estimation, i.e. fewer experiments are needed for the same accuracy as compared to the simple OOS and quantile C_{pk} methods, especially for low number of samples.

In real measurements, only one set of measurements of an EP is available and therefore, it is not possible to determine the accuracy of the estimate and the target is to obtain a low variance of the estimate. However, repeating the same approach for a different EP (with a normal distribution in this case and $FP = 3.55 \cdot 10^{-4}$ considering all measured chips), reveals the inaccuracy of the quantile C_{pk} for low sample sizes. Figure 2.2.9 illustrates the results.

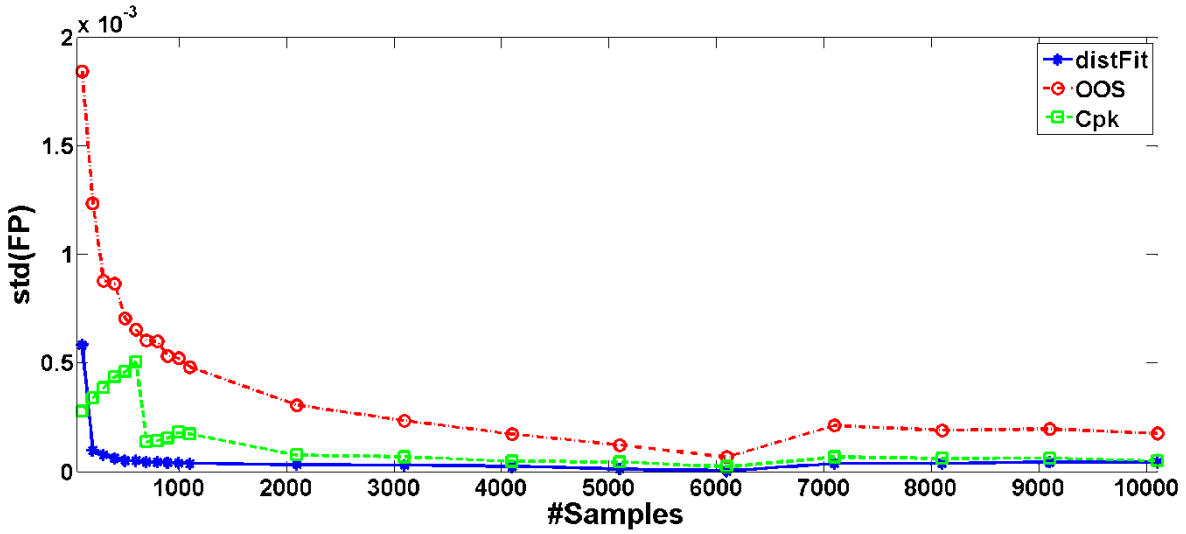

Figure 2.2.8 The standard deviation of the $\boldsymbol{FP}$ using the *distFit*, OOS and equivalent $\boldsymbol{FP}$ of the $\boldsymbol{C_{pk}}$ metrics for one EP with lognormal distribution

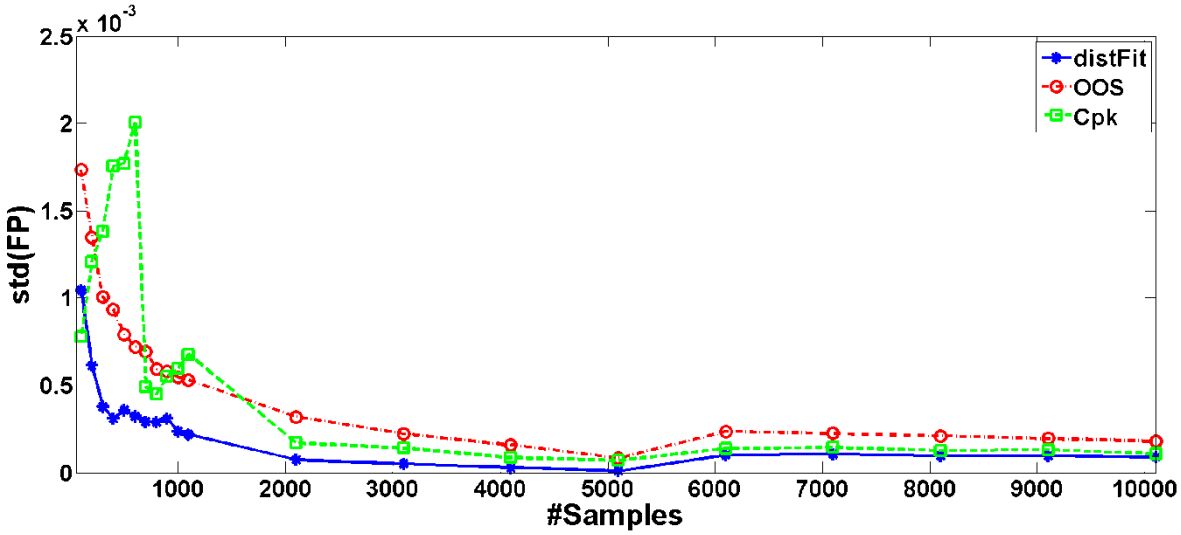

Figure 2.2.9 The standard deviation of the $\boldsymbol{FP}$ using the *distFit*, OOS and equivalent $\boldsymbol{FP}$ of the $\boldsymbol{C_{pk}}$ metrics for one EP with normal distribution

Even if the accuracy of the quantile C_{pk} is comparable to the *FP* using *distFit* and OOS for sample sizes >2000, for samples sizes of a few hundreds (which is a common sample size for measurements at DoE split lots testing phase) the results of the OOS and C_{pk} metrics are rather unreliable and could lead to erroneous decisions about the yield. The DoE split lots or corner lots are groups of fabricated wafers

that have had the process parameters adjusted according to their extreme values and are used to verify the robustness of an integrated circuit design. Practically they are bridging the design phase and mass production phase.

As a final step, the approach for validation of the accuracy of FP using *distFit* over the OOS and quantile C_{pk} metrics was repeated for 25 EPs (including several parametric distributions like normal, lognormal and Gamma). The sample size was $\#Samples = 600$ and again, 1000 subsets of the selected sample size were selected and the standard deviation was computed.

Figure 2.2.10 illustrates an overview of the standard deviation of the FP using the *distFit*, OOS and C_{pk} metrics on several EPs, while in Figure 2.2.11, only the FP using *distFit* and OOS are illustrated for a better comparison.

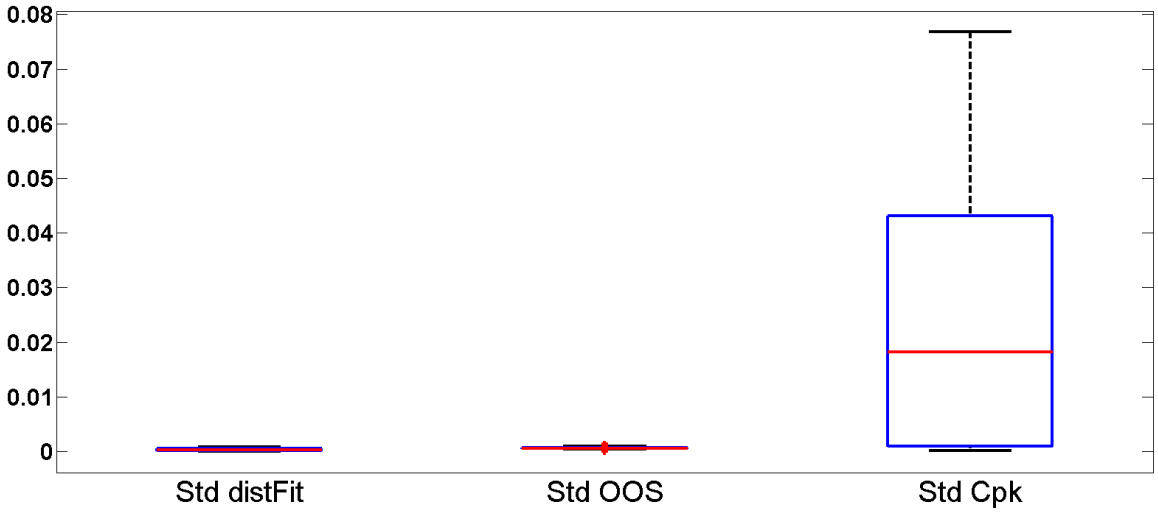

Figure 2.2.10: The standard deviation of the $\boldsymbol{FP}$ using the *distFit*, OOS and C_{pk} metrics on several EPs

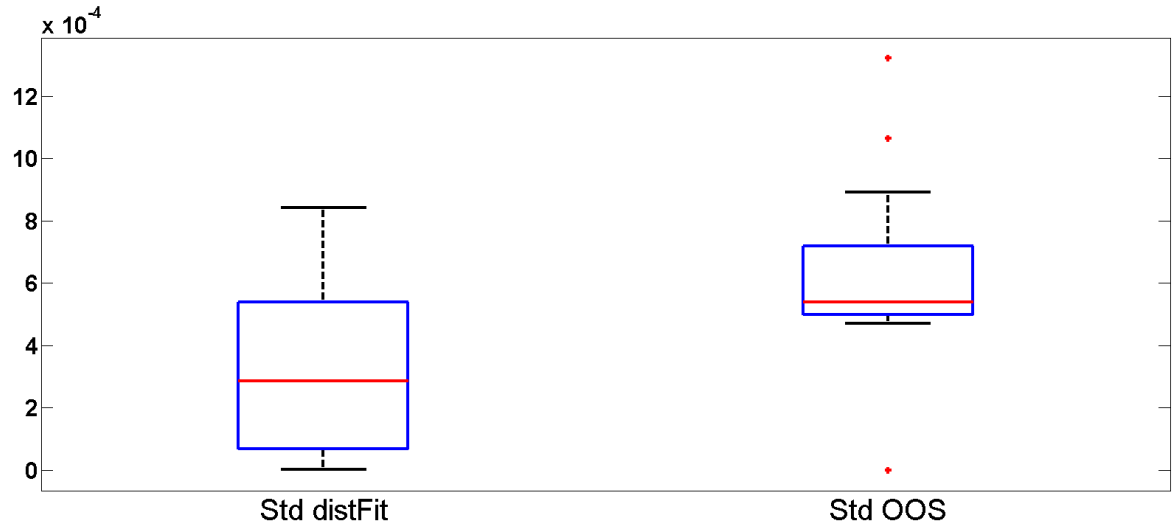

Figure 2.2.11: The standard deviation of the $\boldsymbol{FP}$ using the *distFit* and OOS metrics on several EPs

Comparison of different methods used in yield estimation

In order to show the impact of yield estimation, let's compare the results obtained when using different metrics on data obtained from an intermediate development stage of an IC from the field of

automotive semiconductor industry. The distribution models are used for IC yield analysis and characterization purposes.

The EPs are measured for each chip at different wafers and at different temperatures. Note that there are approximately 200-500 measured chips per each wafer. For the yield analysis purpose, the discrepancies between the proposed FP metric using *distFit*, the OOS counts and quantile C_{pk} were also compared. In the end, the purpose is to determine the metric which gives the most accurate measure of the yield.

The pie chart in Figure 2.2.12 illustrates the statistics of the EPs with critical yield, using FP with *distFit*, OOS and quantile C_{pk} as yield estimation metrics. The targeted yield is the 5 sigma level, which means that an EP is critical if: $C_{pk} < 1.67$; which is equivalent to $FP > 10^{-6}$ and $\mathrm{OOS} > 10^{-6}$. From a total number of ~43000 EPs, 3% are labeled as critical by only one metric while 1% is critical only by the *distFit* metric and the methods agree in 97% of the cases. As expected, there are discrepancies between the metrics and one needs to determine the one that is most accurate.

One further step in the analysis was to inspect the distributions of the EPs with discrepancies, i.e. the EPs which are critical using the *distFit* method, but are not discovered by C_{pk} and OOS metrics. These EPs exhibit a nonparametric distribution in proportion of 97%, while the rest are fit with an extreme value distribution. 2% of the EPs labeled as critical by the quantile C_{pk} or OOS and not critical by the FP using *distFit* have the lowest sample sizes of the data set (around 200 measured chips), a common reason for erroneous conclusions.

The fact that the undiscovered critical parameters had other distributions than normal reveals the importance of using distribution models for IC yield analysis. Indeed, as shown in Figure 2.2.13, only one third of all data was fit with a normal distribution (including also the Box-Cox transformed normal distribution fits) one quarter of the data was fit with other parametric distributions (Gamma, Weibull, extreme value, lognormal), while for the rest the remaining solution was to apply the nonparametric distribution estimation.

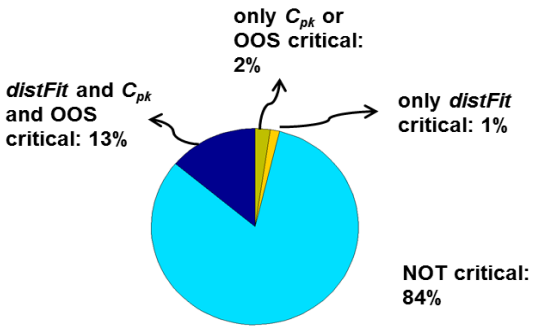

Figure 2.2.12: The statistics of discrepancies between quantile C_{pk}, OOS and *distFit*

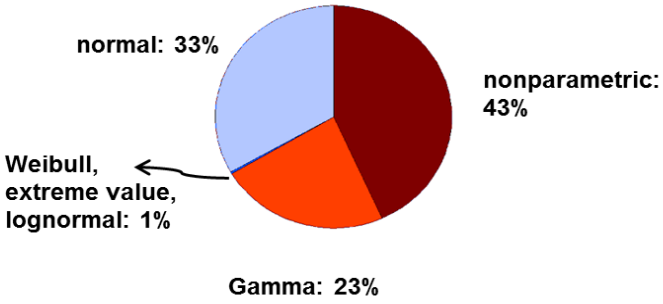

Figure 2.2.13: The distribution statistics of the EPs

2.3 Methods for multivariate yield estimation and figures of merit

Partial yield is the yield calculated from a single output performance parameter. Similarly, the overall yield, i.e. a multivariate yield, can be computed by taking all output performance parameters at once; this is equivalent to the percentage of ICs that meet all specifications (McConaghy et al. 2013). The extent to which the overall yield equals to the partial yield depends on the correlation structure of the output performance parameters. Note that the overall yield is equal to the partial yield if there is a perfect correlation between the output performance parameters; that is, when a chip fails on one output, it also fails on the other and vice versa. On the other hand, if there is no correlation between the output parameters, the overall yield is much lower than the partial yield (McConaghy et al. 2013), more precisely $yield_{overall}=yield_1 \cdot yield_2$. For example, if $yield_1 \cdot = yield_2$=0.90 (i.e. 90%), this leads to an overall yield of only $yield_{overall}$ =0.81. Thus, it is a great challenge to estimate the overall yield, since this is the measure that matters to the design and verification.

- **Multivariate Process capability indices used for multivariate yield estimation**

There is a variety of methods based on the multivariate process capability indices (MPCIs), which usually assume normally distributed data, e.g. MC_p, MC_{pk}, MC_{pm}, MC_{pmk} (Wang and Chen 1998; Che 1994; Taam and Liddy 1993; Shahriari et al. 1995; Xekalaki and Perakis 2002). However, for non-normal data, there is no connection of the MPCI to the yield loss, i.e. if $MC_{pk} = 1$ is equivalent to $C_{pk} = 1$ in the normal case. Moreover, the data is often non-normal and therefore the estimations may be erroneous.

- **Simple count method used for multivariate yield estimation**

The OOS (*Out of Spec*) count is the simplest solution for multivariate yield estimation of non-normal data. However, this metric implies a high variance in estimation and can offer a solid conclusion only if a large number (hundreds of thousands) of samples is available, which in real IC qualification is not affordable.

The OOS method simply counts the number of samples that are inside specification on all outputs and the total number of outputs. This is similar to a binomial approach, where each sample is labelled as pass/fail as illustrated in Table 2.3.1. Note that in Table 2.3.1 a chip represents a sample. $Chip_1$ is an example of failed chip, as it failed the specification compliance at $param_N$. Then, the yield estimate is calculated as the ratio of the two. This approach is troublesome for high-sigma analysis, because for a 5 sigma process, for example, one needs 10^6 samples for consistent conclusions.

Table 2.3.1 The multivariate yield estimation using the *simple count* method

Lot no.	wafer no.	Chip ID	$param_1$	...	$param_N$	Pass/Fail
Lot_1	$wafer_1$	$chip_1$	pass	...	fail	**FAIL**
		...	...	...	...	...
		$chip_K$	pass	...	pass	**PASS**
	$wafer_2$	...	...	...	...	...
...	...	...	...	...	...	...

A solution to overcome the limitation of the OOS would be to generate a high number of samples from the multivariate non-normal and correlated data and apply the OOS metric on it. The literature includes methods of multivariate normal correlated data generation and multivariate non-normal

uncorrelated data generation. However, there are few approaches which combine the two concepts, i.e. generating multivariate non-normal and correlated data (Lange et al. 2016; Guntram 2009).

A direction of research for multivariate data generation is based on the concept of joint distribution modeling using copulas (Naifar 2011; Bounceur et al. 2011). However, the copulas only apply in cases where the marginal distributions are all of the same family, which is a great limitation. Another disadvantage is the high computational time required for the generation of correlated data. Another way is to use the kernel smoothing function, but this has low statistical power.

The proposed methodology for DIstribution model-based Multivariate Yield Estimation (*DIMYE*)

The main problem in yield estimation is the fact that only a small number of samples (chips) is available and the EPs often follow non-normal distributions. The solution proposed in this research is to fit distributions on each EP (Kovacs et al. 2017), followed by the generation of millions of data samples which preserve the statistical properties of each individual EP. However, for the yield analysis, one needs to consider also the correlation structure among the EPs. Therefore, PCA is used to decorrelate the data and fit distributions on each principal component of the PCA space. Then, the inverse transformation is used to return to the initial space. Finally, one only needs to count the failed chips, and this will give a more accurate measure of the yield loss, as it is measured from a much higher number of samples.

Compared to other methods for yield estimation, the proposed approach has the advantage that it uses parametric distributions to generate a high number of random samples of multivariate non-normal and correlated data, which brings an improvement to the accuracy. Unlike the MPCIs, the OOS using the proposed approach directly maps to the yield loss. Another advantage of the proposed method is the compact data storage and representation, which can be further used as input to other analysis.

The DIstribution model-based Multivariate Yield Estimation method (*DIMYE*) aims at using multivariate non-normal distribution models to generate a high number of random samples in each dimension, preserving the distribution in each dimension and the correlation structure among them. Figure 2.3.1 illustrates the idea for two correlated parameters, where the red stars represent the initial data and the green dots represent the high-volume data generated using the *DIMYE* method. In Figure 2.3.1, $F(x)$ denotes the cumulative distribution function (*cdf*) of parameter x. For both parameters, the *cdf* of the initial data is illustrated by the lines with the star markers, while the *cdf* after generating a big number of samples is illustrated by the continuous lines.

Figure 2.3.2 presents the steps of the method. In the first step, the correlated parameters are grouped into clusters. The purpose is to group similar parameters together and also split the data into subsets for easier processing. In the second step, the PCA is applied on each cluster, in order to decorrelate the parameters. The idea is illustrated in Figure 2.3.3, where the principal component space is defined by the direction of the two principal components: PC_1 and PC_2.

In the PCA space, one may apply the univariate distribution fitting methodology on each PC, without needing to consider the correlation structure of the data. In step 4, a high number of samples is generated using the distribution models fitted to each PC. In the last step, the data is transformed from the PCA space to the initial space. The result is data of a much higher sample size that follows the same distribution per each dimension and respects the correlation structure of the data. This idea is presented in Figure 2.3.4, where the stars represent the initial data and the dots represent the data of a big sample size, transformed back from the PCA space.

Note that the correlation structure is preserved. From experiments, the maximum error between the correlation coefficients of the initial and the high-volume data is 0.003.

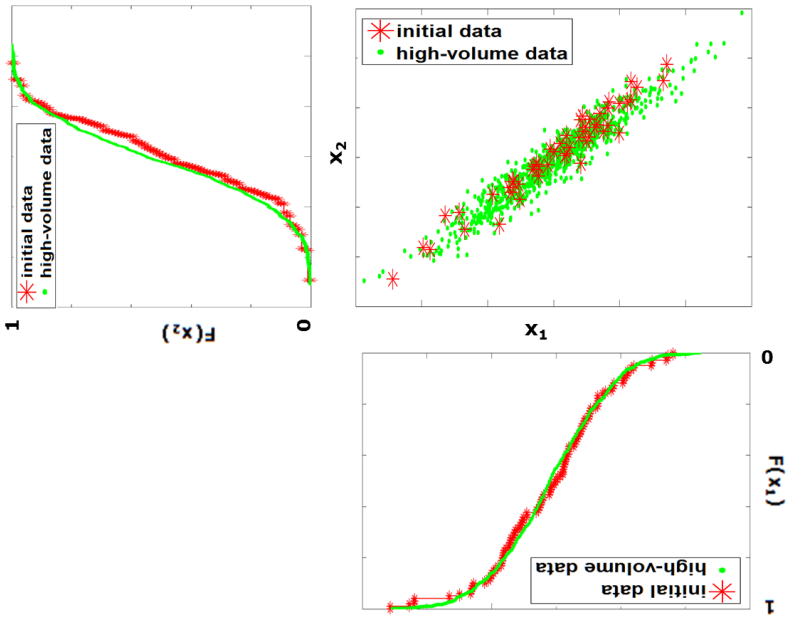

Figure 2.3.1: Illustration of the core idea of the proposed *DIMYE* method

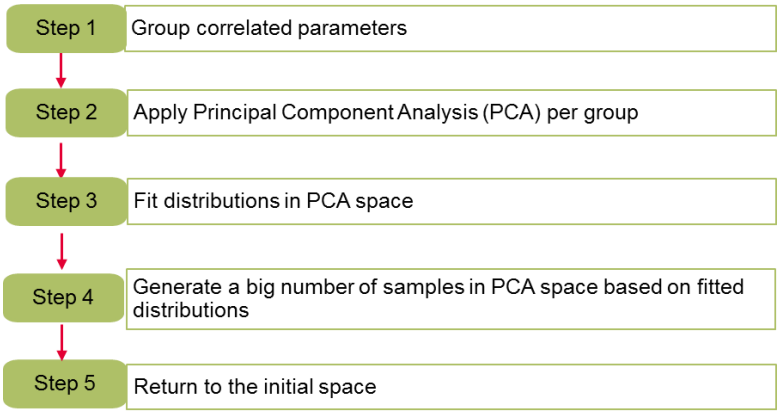

Figure 2.3.2: The steps of the proposed *DIMYE* method

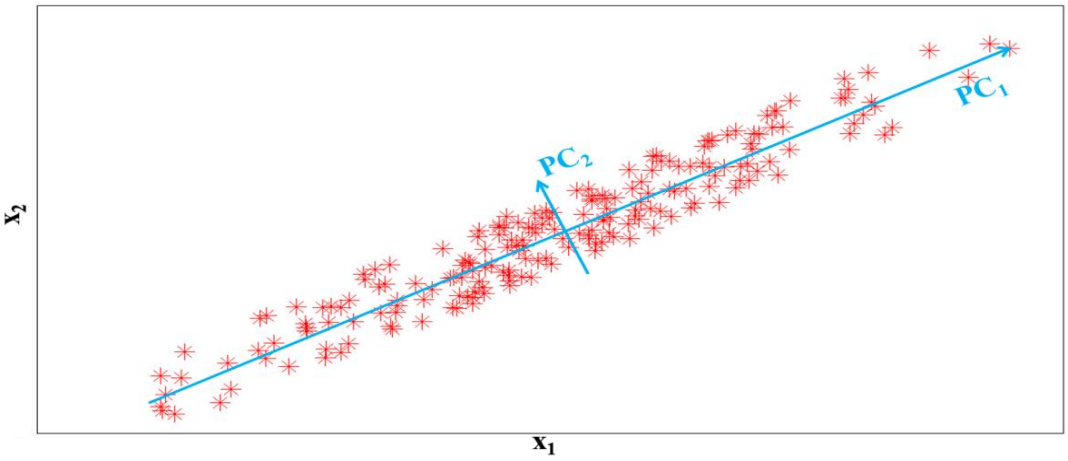

Figure 2.3.3: Illustrating step 2 of the proposed method

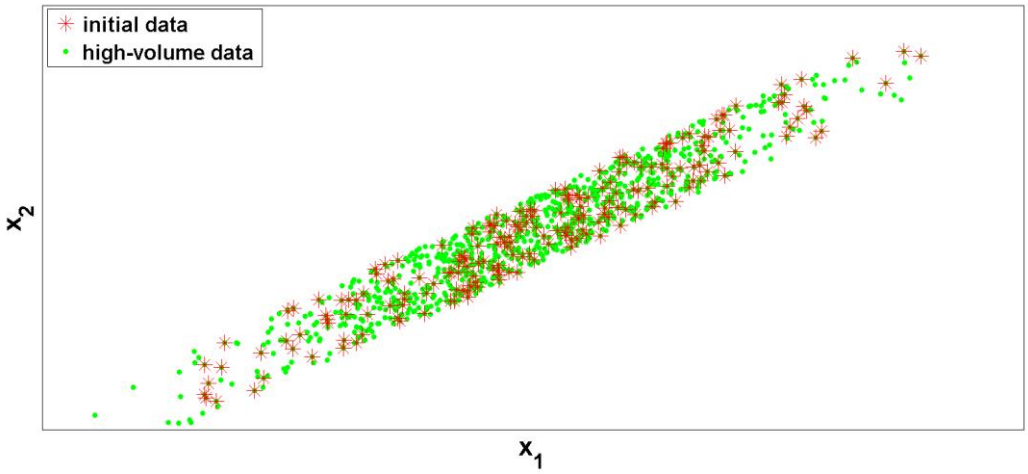

Figure 2.3.4: Illustrating step 5 of the proposed method

For validation purposes, the proposed *DIMYE* method will be applied for the accurate yield estimation of a semiconductor product, for which several EPs were measured, which exhibit non-normal distributions and include also correlations. Note that this data was provided by IFX.

The semiconductor product under investigation was a productive lot including several wafers. A high number (hundreds) of EPs was measured on tens of thousands of chips from these wafers.

Figure 2.3.5 illustrates the distribution statistics of the data. Indeed, only 17% of the EPs follow a normal distribution. Moreover, some EPs are also correlated. Figure 2.3.6 and Figure 2.3.7 present two examples of clusters, built using correlated EPs. Note that EP_1 , ..., EP_4, EP_{10} and EP_{11} generically denote measured EPs.

In order to compare the accuracy of estimation of the simple OOS counts method and the OOS using the *DIMYE* method, the yield loss was estimated from a subset of the available data and it was compared to the yield loss estimated from the lot (considered the ground truth). Using only the subset of the data, the *DIMYE* method was applied to generate a high number of samples (10^6), with the target to have an estimate of the yield loss close to the yield loss of the lot.

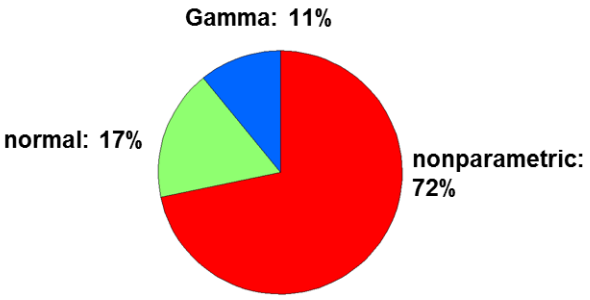

Figure 2.3.5: The distribution statistics of the EPs

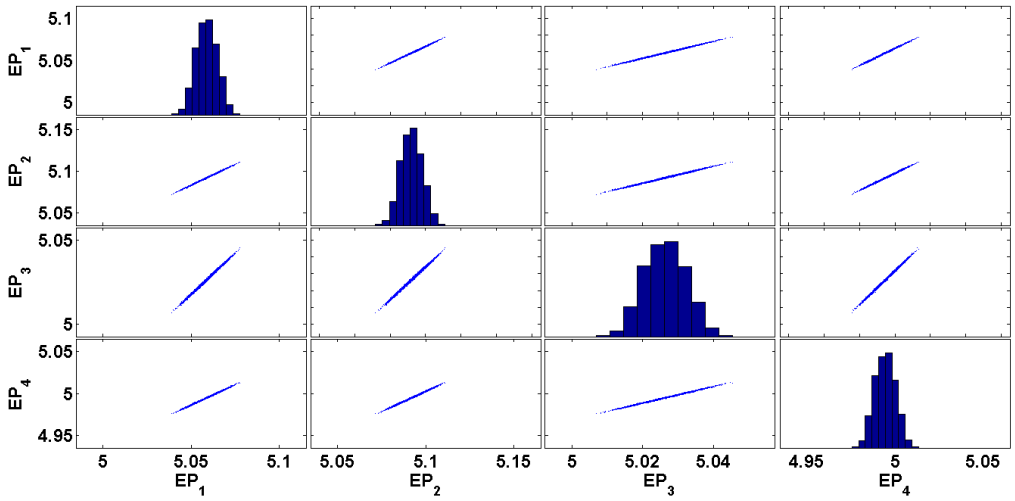

Figure 2.3.6: Example 1 of cluster of correlated EPs

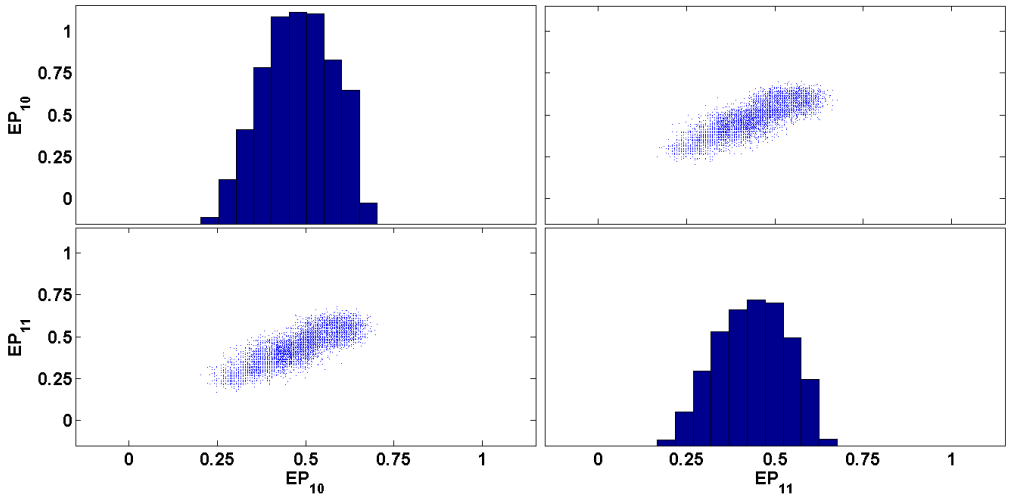

Figure 2.3.7: Example 2 of cluster of correlated EPs

Table 2.3.2 presents a comparison of the yield loss using the measurements from all available wafers and the yield loss predicted by the two methods using only the measurements from $wafer_1$. On this subset of data, the *DIMYE* predicted a yield loss which was closer to the yield loss of the lot than the simple OOS counts method.

In order to determine which method estimates the yield loss with a lower variance, the approach was repeated on all wafers. The box-plots from Figure 2.3.8 illustrate the results. Although the mean value of both metrics is approximately the same and close to the true yield loss of the lot, i.e. 0.34%, the variance of the estimated yield loss using the *DIMYE* approach is two times smaller than the variance from OOS counts, meaning a higher accuracy of estimation.

If one has to discuss about the limitations of the *DIMYE* method, one important issue with the random high-volume sampling in PCA space and transformation back to the initial space is whether the distribution of the data is preserved after the transformation.

From experiments on synthetic data with several parametric distribution types, one can notice that the margins of the distribution after PCA high-volume sampling are slightly different than the distribution of the original data for lognormal and exponential distributions.

Figure 2.3.9 illustrates the results. In

Figure 2.3.9, the red line with the star marker is the original data and the green continuous line is the data obtained after high-volume sampling in PCA space. If the specification limits of these parameters are close to the distribution, this can be a yield detracting fact; otherwise it does not impact the multivariate yield estimate.

Note that in the presented results, no EP had these types of distributions. On the other hand, Figure 2.3.10 illustrates the same idea on a Gamma distribution, where the margins of the distributions are similar.

Table 2.3.2: Yield loss estimation using different yield loss prediction methods (wafer 1)

Yield estimation method	Yield loss [%]
Simple OOS counts considering all wafers	0.34
Simple OOS counts on wafer 1	0.38
OOS counts using *DIMYE* on wafer 1	0.32

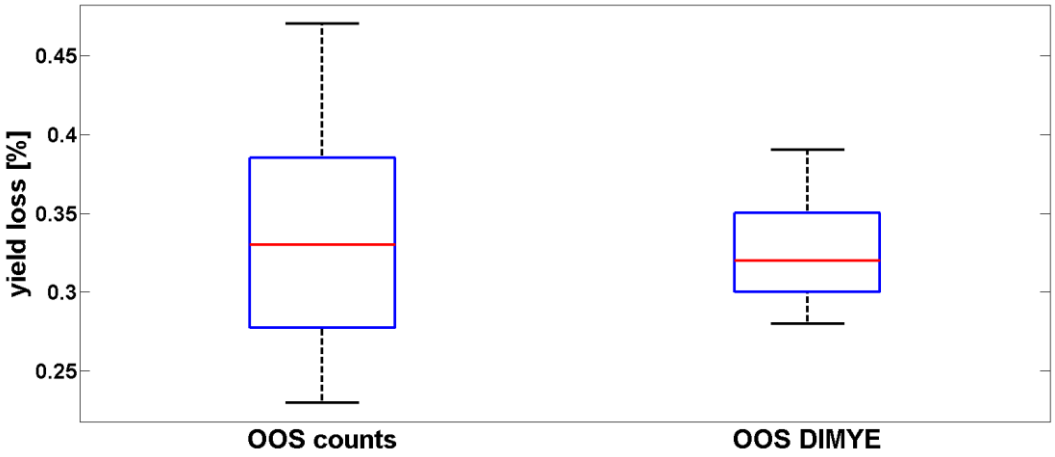

Figure 2.3.8: The variance of estimation of the OOS counts method and the OOS using the DIMYE method

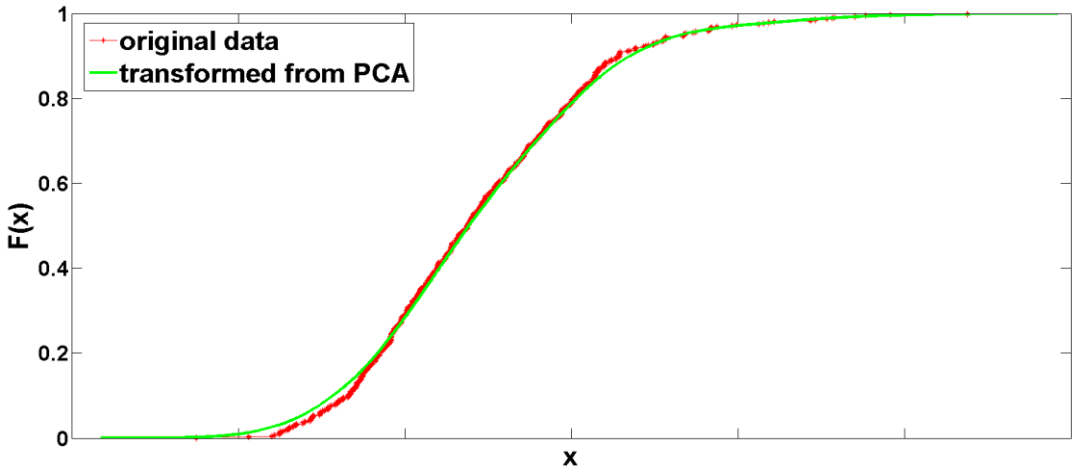

Figure 2.3.9: The *cdf* of the original and transformed data (lognormal distribution)

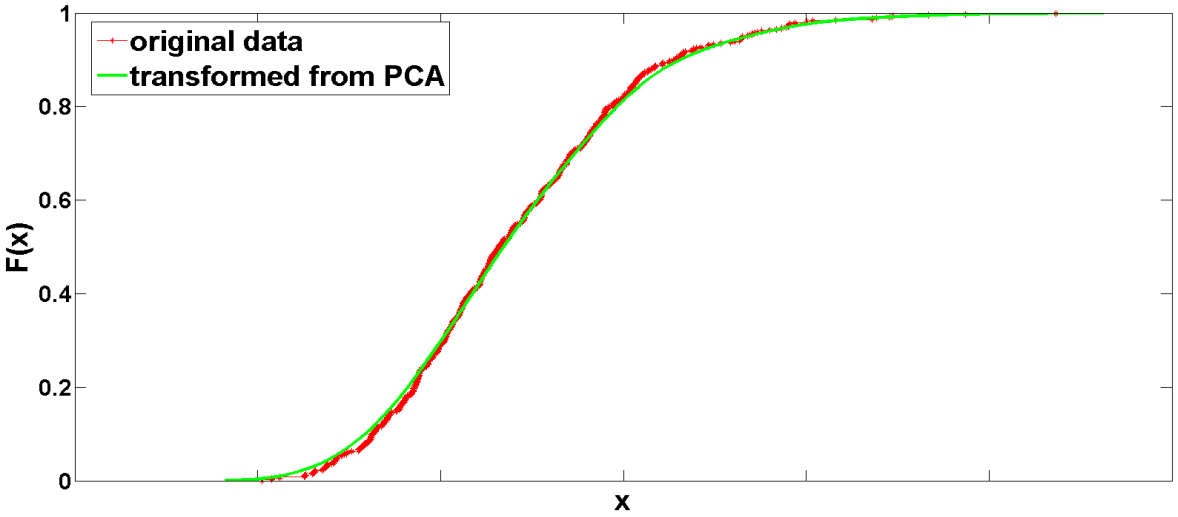

Figure 2.3.10: The *cdf* of the original and transformed data (Gamma distribution)

2.4 Conclusions

This section made an introduction to the yield estimation figures of merit, including metrics of accurate yield estimation in both univariate (yield per electrical parameter) and multivariate cases (yield of the product, i.e. global yield).

Section 2.2 presented methods for univariate yield estimation and figures of merit. Three main categories of figures of merit were described: the simple *out-of-spec* count (OOS) method, methods based on process capability indices and the density-based yield estimation using the failure probability (FP) metric. For most of them, also the confidence interval estimation was described. As at the verification phase of integrated circuits, only a limited number of measurements can be performed, this data represents only a sample from the population. Thus, confidence intervals are suggested to be used; they reflect the degree in which the sample statistic estimates the underlying population.

In Section 2.2,special focus was put on the failure probability (*FP*) metric, which reflects the yield loss based on distribution models, a more robust statistic than the simple *out-of-spec* count or the process capability indices, which usually rely on normal data. Then, validations of the *FP* metric were performed, along with comparison to the performance of other yield estimation methods highly used in verification processes: the *OOS* counts (simple count method) and quantile C_{pk} .The conclusion was that the *FP* metric based on distribution models obtained lower variance in estimation, i.e. fewer experiments are needed for the same accuracy as compared to the simple OOS and quantile C_{pk} methods, especially for low number of samples.

In Section 2.3, we described a distribution model-based multivariate yield estimation (*DIMYE*) method applicable for multivariate non-normal and correlated data. The proposed method used the concepts of clustering and PCA for accurate multivariate yield estimation of semiconductor products.

Then, the proposed *DIMYE* method was applied for the yield estimation of an IC product. The measurements from several wafers from a productive lot were available, which included several electrical parameters, most with non-normal distribution and some correlations among them. Even if this approach of yield estimation was used on the production phase data, this can also be applied in the design phase on pre-silicon MC simulations. In this case the accuracy will depend on the design models and simulated operating conditions accuracy.

In order to compare the accuracy of the estimate obtained using the *DIMYE* method vs. the simple OOS method frequently used for multivariate non-normal data, the yield loss was estimated from a subset of the available data (one wafer at once) and it was compared to the yield loss estimated from

the lot (considered the ground truth). Compared to the OOS counts method, which relies on no statistical information about the data, the proposed method has the advantage of lower variance in estimation.

3 Method for yield detracting factors' determination

3.1 Overview

Besides the yield assessment, one important analysis at IC verification is the yield diagnosis, i.e. identification of the factors leading to yield loss or the so called yield detractors. Moreover, a methodology for yield loss and yield detractors' anticipation brings several benefits, as a long term goal. Most important, it can be useful for preventing redesign and detecting coverage problems.

The current IC verification methodologies offer only a few tools for yield diagnosis and are applied on post-silicon data. Some are based on simple visual inspection of the temperature's and process impact on the distribution of EPs (electrical parameters), others propose the wafer maps' analysis of EPs in order to determine possible yield detracting factors (Kang et al. 2015).

The wafer map is a graphical representation in which the performance of the EP on the wafer is represented by a map as a color-coded grid. This provides intuition about the variation of the performance across the wafer. Thus, trends on wafer may reveal suspicious behaviour of the EP.

Among the simple visual inspection of hundreds of figures, the most frequently used method for yield detractors' analysis is to inspect Pareto charts of the EPs with yield loss (Nist n.d.).

3.2 Method of yield detractors' detection based on process parameters

As a long term goal, one may think of a methodology that is able not only to identify the yield detractors, but also anticipate eventual redesign of an IC product already at simulation. Furthermore, it can be used also for yield optimization purposes. Figure 3.2.1 illustrates the IC verification phases. The criterion of success at the pre-silicon verification is that the predicted yield in simulation is equal to the predicted yield at DoE testing. At the next verification phase, i.e. DoE testing, the criterion of success is that the predicted yield at this phase equals the production yield.

Because of the growing size and complexity of the modern ICs, not all errors may be determined by functional verification on the pre-silicon models. Therefore, the predicted yield at DoE testing may be smaller than the targeted yield. In this case, correcting actions are taken in order to improve the yield. However, if no solution is found, a redesign phase is necessary.

There are several causes for redesign. One first cause is the inaccuracy of the simulation models. More precisely, the models may have unknown parasitic effects or effects that cannot be modeled. Bugs in the tool can also lead to erroneous yield estimation and even redesign.

Another reason for redesign is the low coverage in simulation; there may be bugs that appear in very tight regions of the verification space and remain undiscovered in simulation. Also, one must account for the inherent process variations because they affect the yield. For this purpose, Monte Carlo simulations are performed on the pre-silicon models, while at DoE testing, DoE lots (split lots/corner lots) are inspected. However, the wafers used at DoE testing represent only a snapshot of the process variation, therefore methods are needed that can extract the maximum information from the available results.

This leads to the necessity of an accurate prediction of the yield in pre-silicon verification stage and new methods for yield detractors' identification which enable yield improvement and optimization as early as possible. Also, the correlation between electrical parameters and process parameters has not been investigated in detail yet, although this could be used for yield detractors' anticipation and optimization of the yield itself.

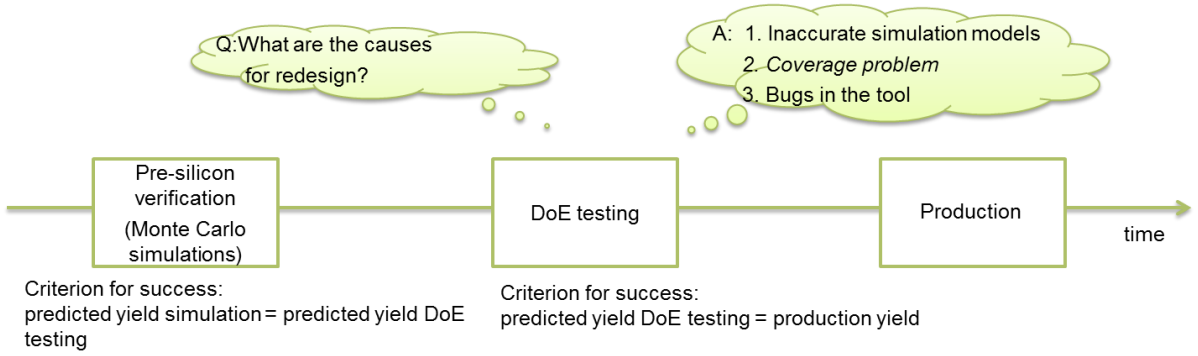

Figure 3.2.1: Illustration of the IC verification phases and causes of yield loss at DoE testing

Figure 3.2.2 illustrates the proposed methodology for the yield detractors' detection based on the correlation of electrical parameters (EPs) and Process control monitor (PCMs) parameters. It is important to highlight hat the proposed method can expose yield loss whenever its root-cause is also reflected by the PCMs. We believe that the information about the correlation of EPs and PCMs can be a simple, but helpful tool for yield detractors' detection and redesign anticipation. Usually, the correlations of PCMs and EPs are intricate and do not have known mathematical expressions, thus statistical methods are needed to capture this effect.

The inputs of the methodology are the PCM data (simulation, DoE testing and production history data) and their specification limits on one hand and the EP data (simulation and DoE testing) on the other hand. The first step of the analysis flow is the data pre-processing step, where EP and PCM data are converted to a unified data structure. Then, the yield per each EP is computed and the EPs with yield loss are detected. Once the EPs with yield loss are identified, the causes need to be detected. Based on the assumption that inaccurate PCM models can be a cause of the yield loss, the correlations of the EPs and PCMs are computed, using simple Pearson correlations (Nist n.d.).

Once the subset of PCMs highly correlated to the EPs of interest are identified, their coverage is checked, i.e. it is inspected whether the variation from post-silicon is fully covered by the variation in simulation. If cases with inaccurate coverage of the PCMs are detected, they are considered to be potential causes of the yield loss, otherwise, the yield loss may be caused by other factors.

The outputs of the analysis flow are summaries of the EPs' yield and their correlations with PCMs in tabular format, but also visualizations like the cumulative distribution function (*cdf*) plots of EPs and PCMs from simulation/ DoE testing and their scatter plots.

This yield detractors' detection approach was tested on an IFX analog IC product data. After the data preprocessing phase, which included the transformation of the data to a MATLAB compatible format, the yield of each EP was inspected in both simulation and DoE testing. Here, the most critical EPs were analyzed, mainly the ones which had yield loss in DoE testing, but no yield loss in simulation. By this, the set of hundreds of EPs was reduced to only a few most critical ones and further analysis was concentrated on these EPs.

Note that the names of both EPs and PCMs are denoted in the following as EP_i and PCM_j, respectively. EP_1 is a first example of EP which had yield loss only in DoE testing. Figure 3.2.3 illustrates the *cdfs* of EP_1 in simulation (blue continuous line) and the 48 wafers from DoE testing, along with the specification limits (red horizontal lines). Note that wafers 47 and 48 have distorted distributions compared to the rest of the distributions and they are also shifted. Also, for accurate coverage, the variation from simulation should cover all variation from DoE. However, for this electrical parameter, the variation in simulation only covers the left side, while the variation of some wafers from the right side is not covered (wafers 39, 40, 47 and 48). This is a first evidence of discrepancy between simulations and measurements.

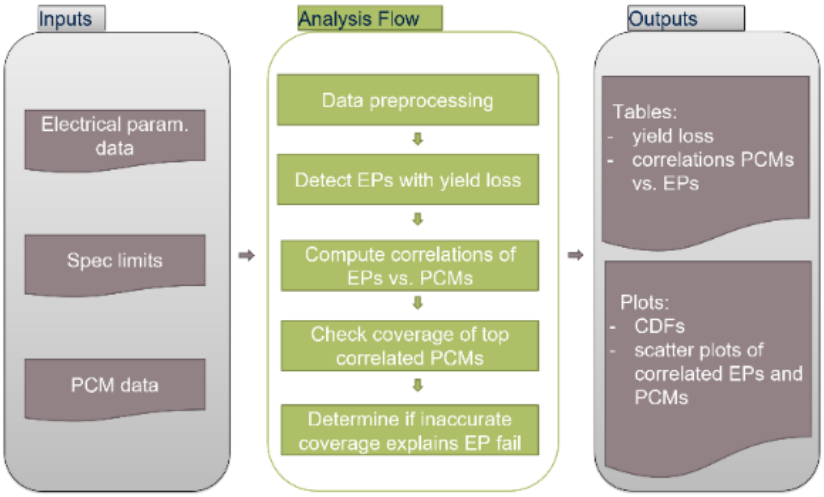

Figure 3.2.2 The yield detractors' detection analysis flow

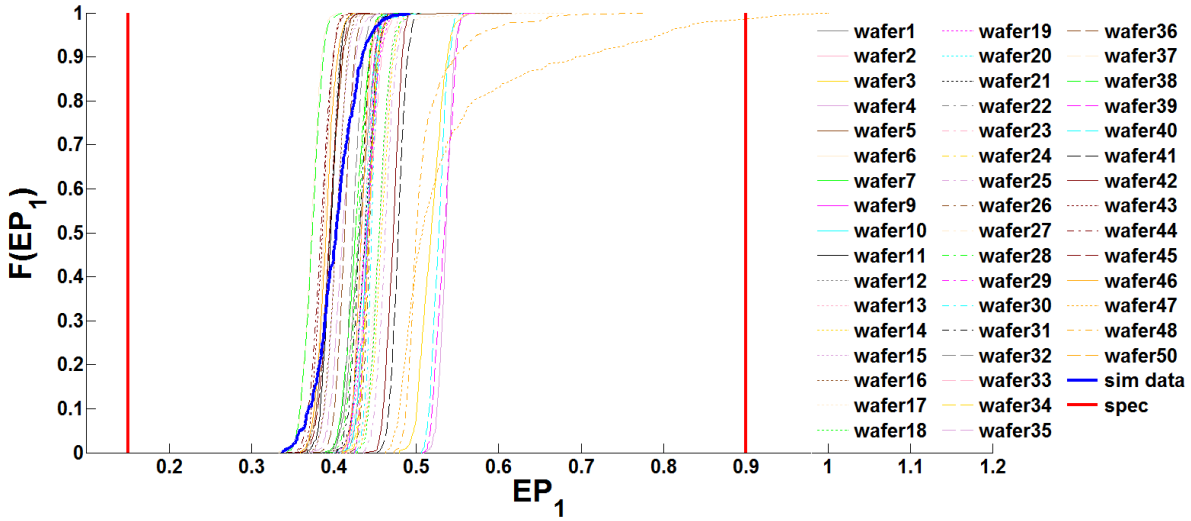

Figure 3.2.3: The *cdfs* of EP_1 in simulation and DoE testing

The box plots from Figure 3.2.4 provide further information about the DoE data per each wafer (x axes) illustrating also the specification limits (red horizontal lines). Note that wafers 47 and 48 have long tail distributions and some measurements fall outside the specification limits.

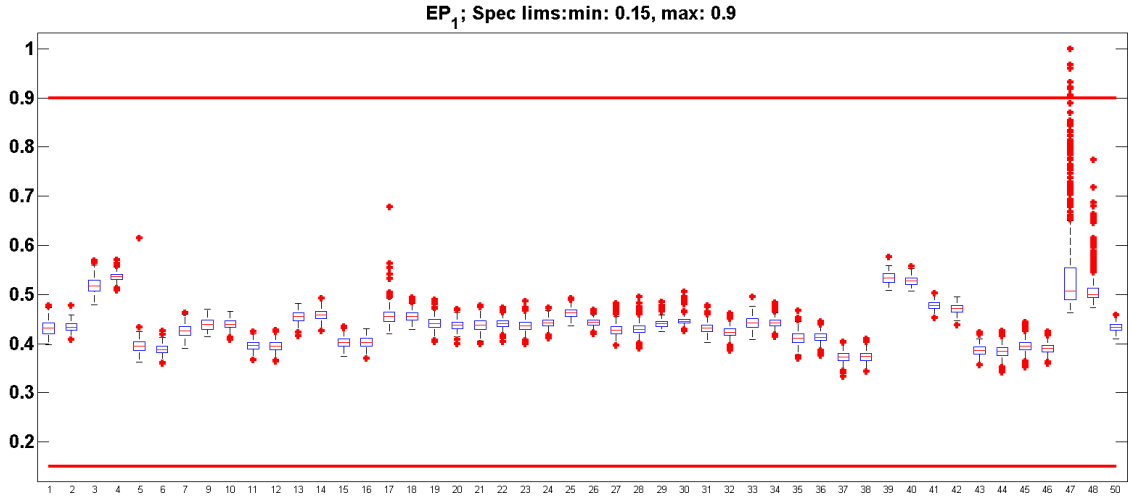

Figure 3.2.4: The box plots of EP_1 in DoE testing

Figure 3.2.5 is an example of electrical parameter, for which the variation in simulation covers all the variation in DoE. This means that this EP is properly modeled.

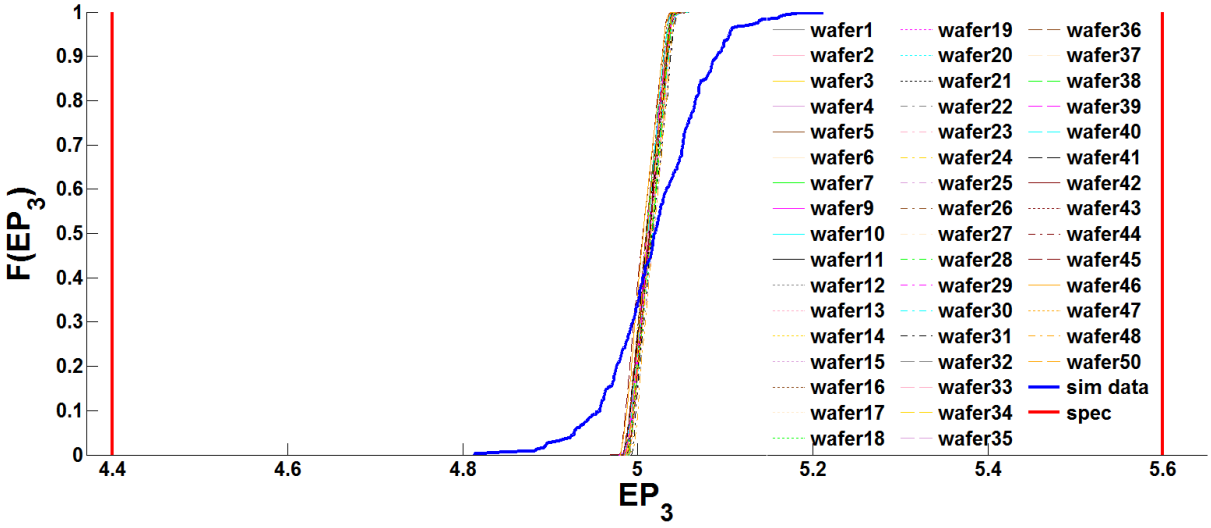

Figure 3.2.5: The *cdfs* of EP_3 in simulation and DoE testing

In order to detect the PCMs highly correlated with EP_1, the Pearson correlation analysis was applied, with the extension of advanced correlations presented in (Pop et al. 2018). The method consists in computing the Pearson correlations on three orders: 1-to-1 correlations of the responses (EPs in this case) with each factor (PCMs in this case), the correlations of the responses with the product of each pair of factors, respectively, the correlations of the responses with the product of each triplet of factors. The top of the most relevant PCMs is returned, by ranking the normed-weighted scores of the PCMs based on correlation coefficients computed on these three orders.

Note that the correlation analysis was applied on the mean values per wafer of both EPs and PCMs. Table 3.2.1 presents the top of the most correlated PCMs to EP_1. Note that the PCM names, as also the EPs, are anonymized.

Then, the distributions of PCMs were inspected in order to check if the variation of the PCM models cover the variation in DoE testing. As there were only a few PCM measurements per wafer, all measurements were cumulated to build a distribution in DoE testing. Moreover, some PCM measurements were available from earlier measurements of IC products from the same technology, so this data was used to represent the history data of the PCMs.

Figure 3.2.6 - Figure 3.2.7 depict the *cdfs* of some PCMs in simulation vs. DoE testing vs. history, which are also included in the correlation table from Table 3.2.1. From Figure 3.2.6, it can be noticed that the variation of PCM_1 in simulation fully covers the variation in DoE testing. Moreover, its distribution did not shift compared to the history data.

Table 3.2.1: Top weighted correlation scores of PCMs vs EP_1

Ranking	PCM names	Score
1.	PCM_1	0.70
2.	PCM_2	0.61
3.	PCM_3	0.53
4.	PCM_4	0.53
5.	PCM_5	0.50
6.	PCM_6	0.50
7.	PCM_7	0.50
8.	PCM_8	0.50

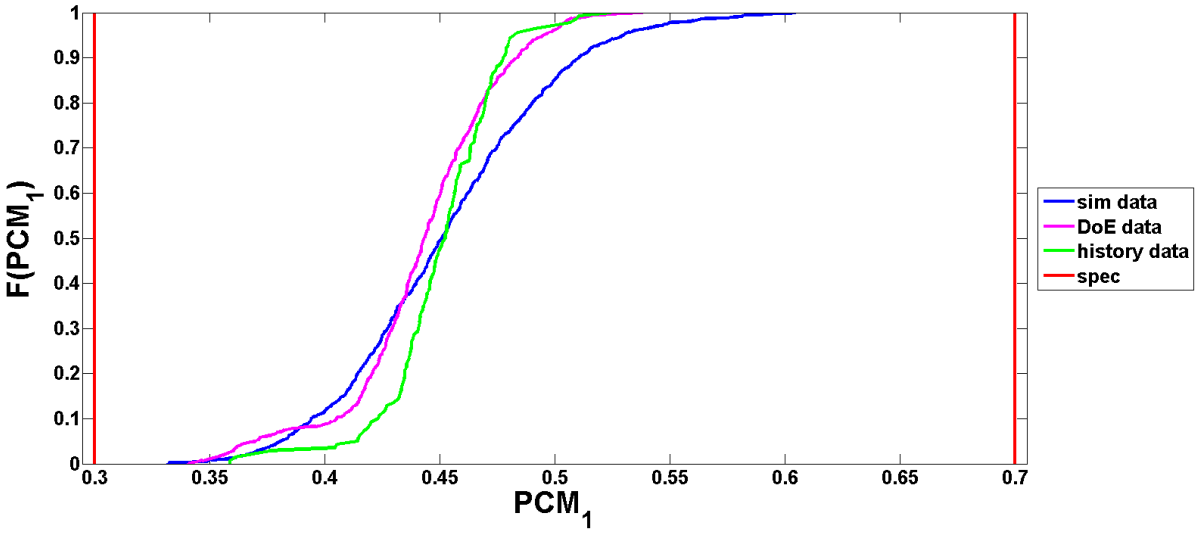

Figure 3.2.6: The *cdfs* of PCM_1 in simulation vs. DoE testing vs. history

Figure 3.2.7 illustrates the *cdfs* of PCM_2 in simulation vs. DoE testing vs. history. Note that there is a shifting of the distribution of PCM_2. This time, the variation in simulation does not cover the variation in DoE testing. The rest of the PCMs correlated to EP_1 (PCM_3, PCM_4, PCM_5, PCM_6, PCM_7 and PCM_8) describe similar cases as the ones described by PCM_1 and PCM_2.

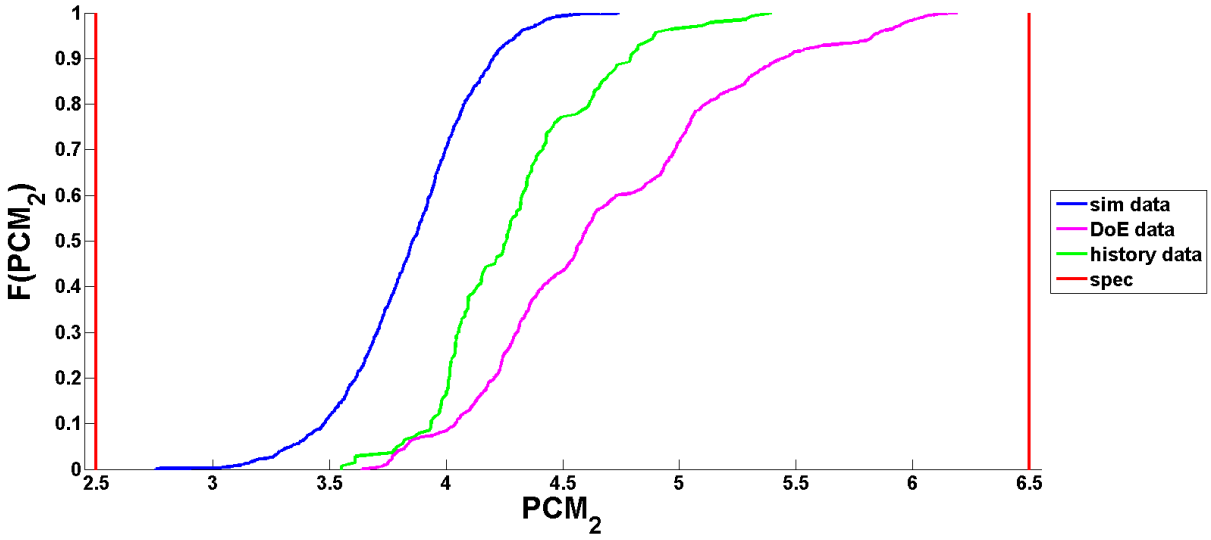

Figure 3.2.7 The *cdfs* of PCM_2 in simulation vs. DoE testing vs. history

Figure 3.2.8 - Figure 3.2.9 illustrate the box plots of several PCMs included in the Table 3.2.1. Using the box plots, one can visualize how these PCMs were varied on each wafer individually. Note that PCM_1 was not varied much from one wafer to the other (see Figure 3.2.8). On the other hand, PCM_2, for example, is shifted to high values on wafers 17, 18 and 47 and 48 (see Figure 3.2.9).

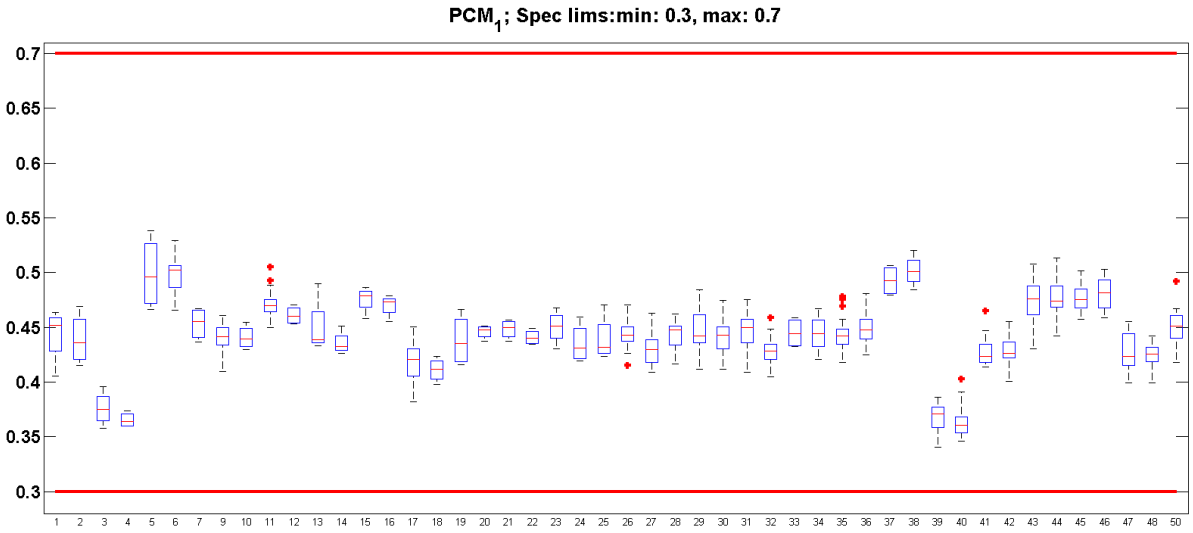

Figure 3.2.8: The box plots of PCM_1 in DoE testing

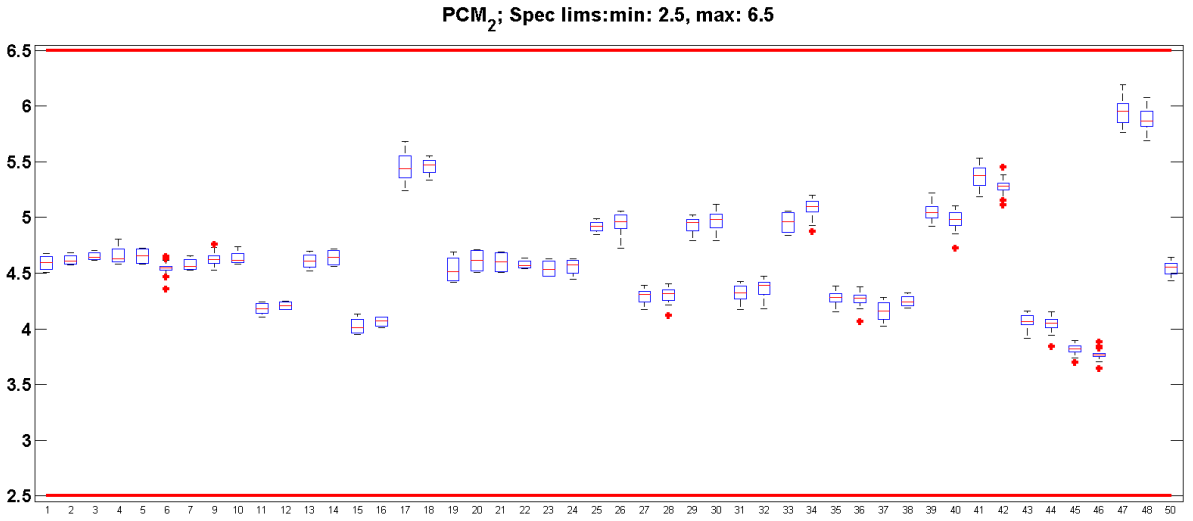

Figure 3.2.9: The box plots of PCM_2 in DoE testing

The analysis of the eight PCMs (their *cdfs* and box plots) lead to the conclusion that only PCM_2 had coverage problems and was also varied on the wafers on which the EP_1 had yield loss or distorted distributions. Thus, it is of interest to make further investigations on PCM_2 and determine if the yield loss of EP_1 can be explained by the inaccurate coverage of PCM_2.

Figure 3.2.10 illustrates the scatter plot of EP_1 vs. PCM_2, where each marker (o, *, +, etc) represents a wafer (the mean value of the EP or PCM on it), and the red rectangle is formed by the specification limits. Note that wafers 47 and 48, depicted with the orange circle and diamond markers, are the most extreme values of both PCM_2 and EP_1. For a better visualization, Figure 3.2.11 illustrates the two wafers with yield loss in different color (cyan diamond) than the rest of the wafers.

Note that PCM_2 has also a quadratic effect on EP_1. The 3-dimensional plot from Figure 3.2.12 illustrates this. Note that, again, the two wafers which had yield loss can be detected easily and for these, the EP exhibits the highest values (see Figure 3.2.13).

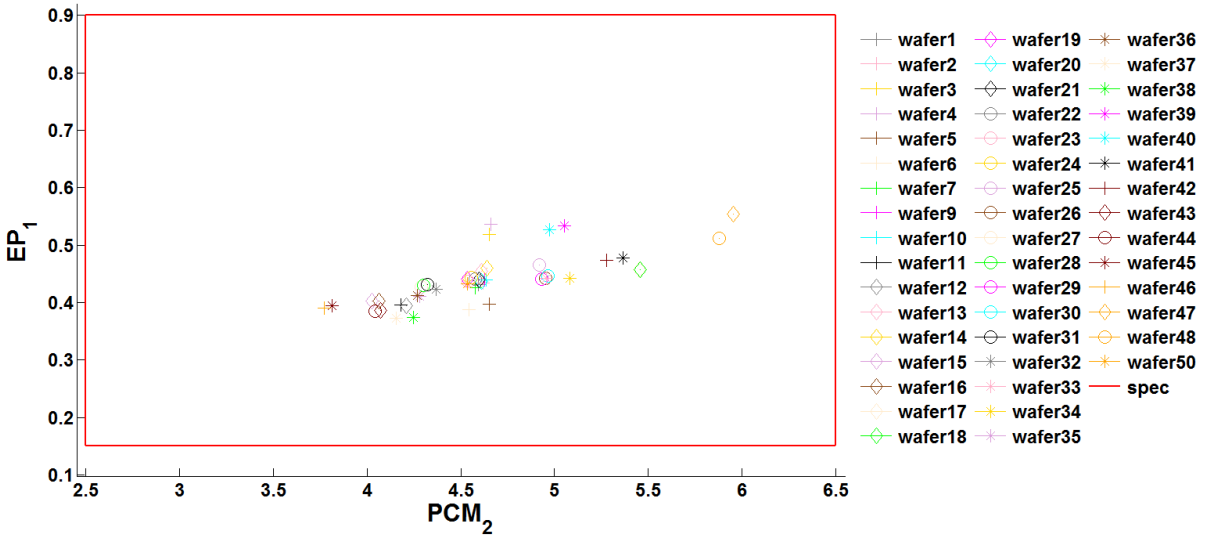

Figure 3.2.10: Illustrating the first order effect of PCM_2 on EP_1

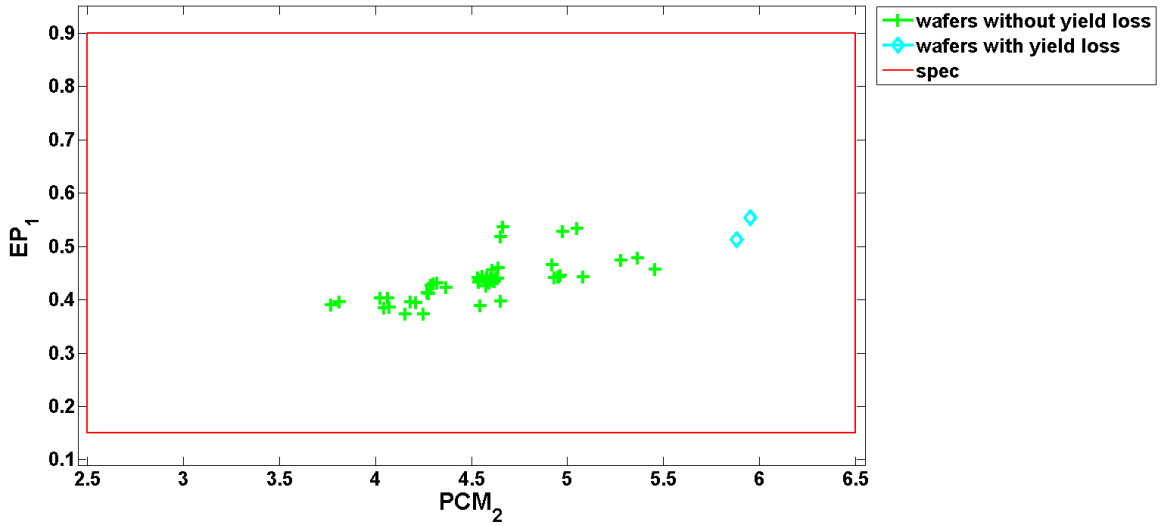

Figure 3.2.11: Illustrating the first order effect of. PCM_2 on EP_1 (wafers with yield loss highlighted)

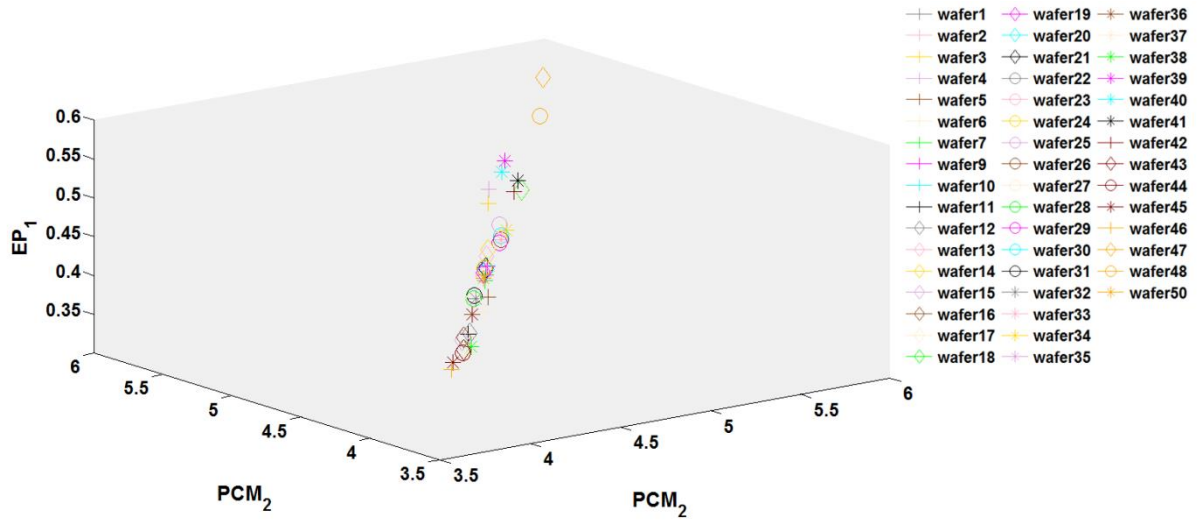

Figure 3.2.12: Illustrating the quadratic effect of PCM_2 on EP_1

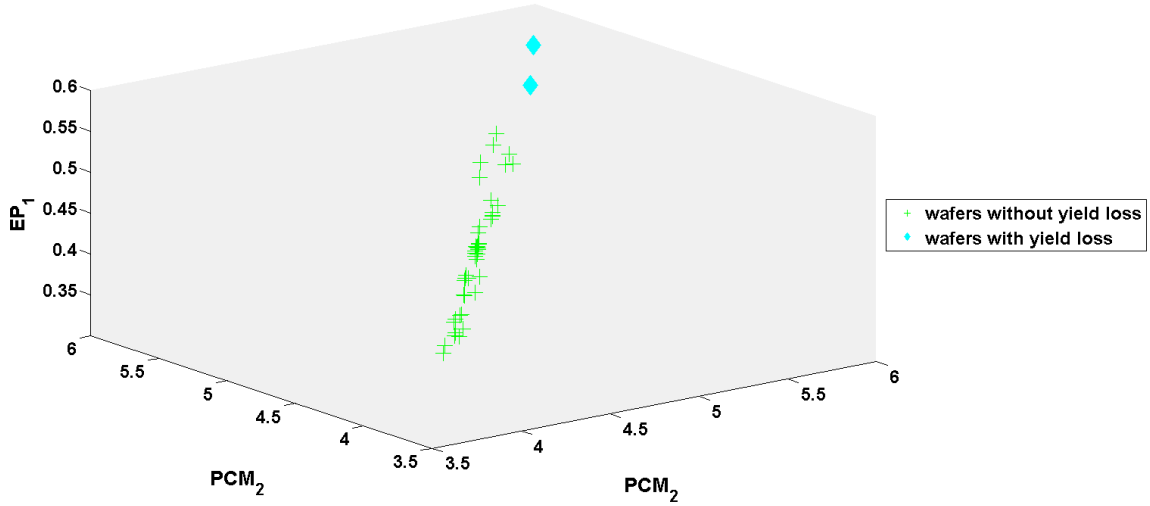

Figure 3.2.13: Illustrating the quadratic effect of PCM_2 on EP_1 (wafers with yield loss highlighted)

3.3 Conclusions

This chapter mainly focused on yield detractors' detection approaches. The first part of it briefly described the current approaches for yield detractors' analysis, such as the inspection of wafer maps and Pareto charts analysis.

The second part of this chapter described the development of a method for yield detractors' detection and anticipation, based on the correlation information of electrical parameters (EPs) and process control monitors (PCMs).

The approach was tested on an IFX IC data. Using the proposed methodology, the set of PCM parameters was reduced to only one PCM parameter which had coverage issues, i.e. its variation in simulation did not cover its variation from DoE testing. Moreover, the PCM was also correlated to the EP which had yield loss, proving that its coverage issue was a yield detracting factor. IFX designers also confirmed the identified yield detracting PCM. The conclusions of the methodology are conditioned by the assumption that the circuit device models reflect reality with high precision.

This approach can be used in the design phase, before mass production and can be used by circuit designers to redesign the circuit in order to provide increased robustness to the technology variations associated to the yield detracting PCMs.

Future work includes the development of methodologies that contribute to yield optimization and accurate yield prediction in simulation by using the correlation information between the electrical parameters and process parameters.

4 List of Abbreviations

Abbreviation	Meaning
cdf	cumulative distribution function
CI	Confidence Interval
EP	Electrical Parameter
FP	Failure Probability
IC	Integrated circuit
LSL	Lower Specification Limit
MPCI	Multivariate Process Capability Index
OOS	Out-of-Spec count
PCI	Process Capability Index
PCM	Process Control Monitor
pdf	probability density function
USL	Upper Specification Limit

5 References

Agresti, A. and Coull, B. A. (1998): Approximate is better than "exact" for interval estimation of binomial proportions, in: The American Statistician, vol. 52(2), 119-126.

Bounceur, A., Mir, S. and Stratigopoulos, H.G. (2011): Estimation of analog parametric test metrics using copulas, in: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 30, no. 9, pp. 1400–1410.

Box, G.E. and Cox, D. (1964): An analysis of transformations: Applying the Box-Cox transformation, in: Journal of the Royal Satistical Society, Series B, vol. 26, pp. 211–252.

Brown, L.D., Cai, T. and DasGupta A. (2001): Interval estimation for a binomial proportion", Statistical Science, vol. 16, no. 2, pp. 101-13

Chen, K.S., Pearn, W.L. and Lin, P.C. (2003): Capability measures for processes with multiple characteristics, in: Quality and Reliability Engineering International, vol. 19, no. 2, pp. 101-110.

Che, H. (1994): A multivariate process capability index over a rectangular solid tolerance zone", in: Statistica Sinica, vol. 4, pp. 749-758.

Clements, J.A. (1989): Process capability calculations for non-normal distributions, in: Qual. Progress, vol. 22, pp. 95–100.

McConaghy, T., Breen, K., Dycke, J., Gupta, A. (2013): Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide, [online] http://doi.org/10.1007/978-1-4614-2269-3.

Guntram, E. (2009): A general yield model from design to product engineering, in: IEEE Transactions on Semiconductor Manufacturing, vol. 22, no. 3, pp. 536-543.

Kang, S., Cho, S., An, D. and Rim, J. (2015): Using Wafer Map Features to Better Predict Die-Level Failures in Final Test, in: IEEE Transactions on Semiconductor Manufacturing, vol. 28, pp. 431–437.

Kotz, S. and Johnson, N.L. (2002): Process capability indices – a review, 1992–2000, in: Journal of Quality Technology, vol. 34, no. 1, pp. 1–19.

Kotz, S. and Johnson, N.L. (1992): Distributional and inferential properties of process capability indices, in: Journal of Quality Technology, vol. 24, no. 4, pp. 216–231.

Kovacs, I, Topa, M., Buzo, A., Pelz, G. (2017): Integrated Circuits' Characterization for Non-normal Data in Semiconductor Quality Analysis, in: IEEE European Test Symposium (ETS), Limassol, Cyprus, pp. 1-2.

Lange, A. et al. (2016): Multivariate modeling of variability supporting non-gaussian and correlated parameters, vol. 35, no. 2, pp. 197–210.

Naifar, N. (2011): Modelling dependence structure with Archimedean copulas and applications to the iTraxx CDS index, in: Journal of Computational and Applied Mathemematics, vol. 235 no. 8, pp. 2459–2466.

Nist (n.d.): NIST/SEMATECH, The e-Handbook of National Institute of Standards and Technology (NIST), [online] http://www.itl.nist.gov/div898/handbook/NIST.

Pearn, W.L., Lin, G.H. and Chen K.S. (1998): Distributional and inferential properties of the process accuracy and process precision indices, in: Communications in Statistics: Theory and Methods, vol. 27, no. 4, pp. 985–1000.

Pop, C., Buzo, A., Pelz, G., Cucu, H., Burileanu, C. (2018): Methodology for determining the influencing factors of lifetime variation for power devices, in: IEEE European Test Symposium (ETS), pp. 1-2.

Shahriari, H., Hubele, N., Lawrence, F. (1995): A multivariate process capability vector, in: Proceedings of the 4th Industrial Engineering Research Conference, vol. 1, pp. 304-309.

Taam, W. SP. And Liddy, JW. (1993): A note on multivariate capability indices, in: Journal of Applied Statistics, vol. 20, pp. 339-351.

Wang, F. and Chen, J. (1998): Capability index using Principal Components Analysis, in: Quality Engineering, vol. 11, no. 1, pp. 21–27.

Wildon, E.B. (1927): Probable inference, the law of succession and statistical inference, in: Journal of American Statistical Association, vol. 22, pp. 209-212.

Xekalaki, E. and Perakis, M. (2002): The use of principal component analysis in the assessment of process capability indices, in: Proceedings of the Joint Statistical Meetings of the American Statistical Association, The Institute of Mathematical Statistics, The Canadian Statistical Society, New York.

Zhang, N.F, Stenback, G.A. and Wardrop, D.M. (1990): Interval estimation of the process capability index, in: Communications in Statistics: Theory and Methods, vol. 19, no. 21, pp. 4455-4470.