D7.3

Report on virtual prototyping rules for DFM Optimization

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Publishable Executive Summary

This deliverable focuses on the activity performed in tasks **T7.1.2** (Virtual investigations of test boards), **T7.2.1** (Design Methodology for Reliability Analysis and Yield Prediction) in the direction of reliability analysis and **T2.4.1** (Methodology for Reliability Analysis and Yield Prediction). The above-mentioned activities are related to **Use Case 4** (IC yield prediction with knowledge-based modelling) (Lead: IFRO) and succeeds deliverable **D7.7** (Efficient Modelling of Electro-Thermo-Mechanical Stress During Fast Power Cycling Operation of an IC).

The deliverable is structured in three chapters, followed by conclusions:

- Chapter 1 is an introduction and presents the scope of the work and partners involved.
- Chapter 2 presents the complete design flow of an electronic product – from the idea to the mass production and continues with the description of key IPC (Association Connecting Electronics Industries) standards that need to be considered when performing the design for manufacturing (DFM); additionally, some of the most important DFM issues are described.
- Chapter 3 focusses on the principles of PCB footprints design for DFM for Surface Mount Technology (SMT) and Through-Hole Technology (THT) required for an optimal manufacturing process.

The activity in task **T7.1.2** has started in January 2020 due to delays in the release of funds by the Romanian funding authority and the necessity to re-align the activity with the current situation of the activities at project level.

The activity in task **T7.2.1** has started in December 2019 due to delays in the release of funds by the Romanian funding authority.

The activity in task **T2.4.1** related to the simulation of stress in matching device pairs has started in December 2019.

This deliverable contributes to the following objectives of the project:

- Objective 7.1 (WP7) – Task 7.1.2, virtual investigations of test boards and Task T7.2.1, design methodology for reliability analysis and yield prediction.
- Objective 1.2 (WP1) - Task T1.2.1, upgraded virtual prototyping requirements.
- Objective 2.4 (WP2) – Task 2.4.1, methodology for reliability analysis and yield prediction.

The deliverable supports the objectives oriented to increase the level of virtual prototyping and to minimize the design and manufacturing loop iterations at the project partner IFRO for a test board designed for parallel testing of ICs in fast thermal cycling conditions.

Key Words

Design For Manufacturing (DFM); virtual prototyping rules; optimization; thermal management design rules

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1 Introduction

The present deliverable focuses on activities performed in tasks **T7.1.2** (Virtual investigations of test boards), **T7.2.1** (Design Methodology for Reliability Analysis and Yield Prediction) in the direction of reliability analysis and **T2.4.1** (Methodology for Reliability Analysis and Yield Prediction) and aims to structure and present the virtual prototyping rules for Design for Manufacturing (DFM) optimization of the electronic test boards designed and used to analyse the reliability of integrated circuits developed within the iDEV40 project. The above-mentioned activities are related to **Use Case 4** (IC yield prediction with knowledge-based modelling, lead: IFRO) and succeeds deliverable **D7.7** (Efficient Modelling of Electro-Thermo-Mechanical Stress During Fast Power Cycling Operation of an IC).

The work focuses on the Design For Manufacturing (DFM) concept, a concurrent engineering set of techniques developed to bring the down-stream life-cycle product concerns to the forefront of the design process, to optimize the future product early in the concept & design phase in order to ensure that the product will be manufactured in the most efficient possible way. In this process, the design of product is optimized, being modified to fit the capabilities of the manufacturing facilities. The optimization is done by applying DFM principles described in the following chapters according to international standards developed and governed by IPC (Association Connecting Electronics Industries), using standard components, eliminating unnecessary devices, integrating multiple components, selecting easy to assemble components and parts, etc. These procedures will not only create a product easy to be manufactured, but also one that uses less material, is of a better quality and involves lower costs, giving to companies a competitive advantage in today's world market.

The team from University Politehnica of Bucharest (UPB) is part of the Faculty of Electronics, Telecommunications and Information Technology, Center for Technological Electronics and Interconnection Techniques (CETTI) and focuses on advanced CAD-CAE-CAM, design for manufacturing and advanced virtual investigations of electronics modules.

Within **task T7.1.2** UPB is performing advanced virtual investigations of test boards developed by the project partner IFRO. The set goal is to increase the level of virtual prototyping and to minimize the design and manufacturing loop iterations.

Within **task T2.4.1** IFRO has developed an extension of the existing simulation flow to accommodate the requirements of IFAT for simulation of mechanical stress. This extension is then used by IFAT for performing simulations of various scenarios, which are used for deriving the DFM design rules presented in this deliverable.

After this introduction, the deliverable is structured in two chapters. Chapter 2 presents the entire design flow of an electronic product, from the idea to the mass production and key DFM issues that need to be considered when designing for manufacturing. It offers details about the spacing between components, fiducial markers, thermal reliefs, solder thieves (ST) in case of wave soldering and recommendation for optimizing a design for increased thermal efficiency. Chapter 3 is dedicated to the principles of PCB footprints design for DFM, in order to match both the Surface Mount Technology (SMT) and Through Hole Technology (THT). At the end of the deliverable, a set of unified conclusions is presented.

The activity within the two tasks which is not presented in this deliverable or which will take place in the final year of the project will be included in deliverables D2.16 (IC Design Methodology based on multi-physics modelling and simulation) and D7.8 (Methodology for electro-thermo-mechanical simulation).

Regarding introduction of Design For Manufacturing (DFM) concept and principles, electronic products can be found today in all areas of the life (consumer, telecommunications, infrastructure, IT, medicine, aeronautics, automotive, etc.). Their development is based on electronic packaging, which is a major discipline within the field of electronics engineering, including a wide variety of techniques and technologies for conception, design, manufacturing and testing of electronic modules and systems (products, in general) (Codreanu 2009).

Electronic products are complex entities composed of numerous active and passive components, assembled on one or multiple printed circuit boards (PCB) and interconnected to achieve specific functions (Codreanu 2009; Coombs and Holden 2016).

In the last two decades, more and more concepts, as Design For Manufacturing (DFM), Design For Assembling (DFA), Design Of Experiments (DOE), Design For Testing (DFT) (Blackwell 2000), Design For Environment (DFE), etc. were implemented in order to obtain products with increased quality and reliability. The PCB design has proven to have a major influence on the manufacturing, assembling, and testing processes (Blackwell 2000) and all the concepts from above try to establish design rules that lead to a better-quality product.

The design of high-quality electronic modules/systems is based on the DFM concept, which is a complex set of rules and principles for performing conception, design and post-processing activities focused on the real manufacturing. DFM integrates manufacturing and optimization principles into the early stages of the development of electronic products. Today, the design flow of any electronic product is based on the fundamental set of acronyms CAE-CAD-CAM (Computer Aided Engineering - Computer Aided Design - Computer Aided Manufacturing), which defines all the development stages during the conception, design, manufacturing and testing of electronic modules/systems (Codreanu 2009).

A design flow is a guide for turning a concept into a real working product, flow which can be based on a unique CAE-CAD-CAM environment or on various different environments, correlated to offer a proper solution for analogue, digital and mixed-signal schematic design, circuit simulation, layout design and optimization, design rules check, and DFM/CAM features for interfacing with the manufacturer (Elect2eat 2007; Msystech 2009). The design flow implements a gradual transition from idea to final, real electronic module/system. The flow is generally defined by the following steps (Elect2eat 2007; Coombs and Holden 2016):

1. Conception stage;
2. Schematic design, which turns a block diagram into a detailed schematic diagram;
3. Schematic optimization;
4. Schematic post-processing;
5. Circuit simulation and upgrade of the schematic design, if necessary;
6. PCB layout design, the process of transforming a schematic diagram into a printed circuit layout;
7. DFM and layout optimization;
8. PCB layout post-processing, which creates a set of post-processing files suitable for manufacturing;
9. Signal & power integrity analysis and electromagnetic compatibility investigations;
10. Other optimizations of the PCB layout design, if necessary;
11. Interfacing the design with the specific manufacturing facilities.

Finally, the design flow can be integrated in a larger and complete flow, consisting in all the stages involved in the development and introducing new electronic products into the market.

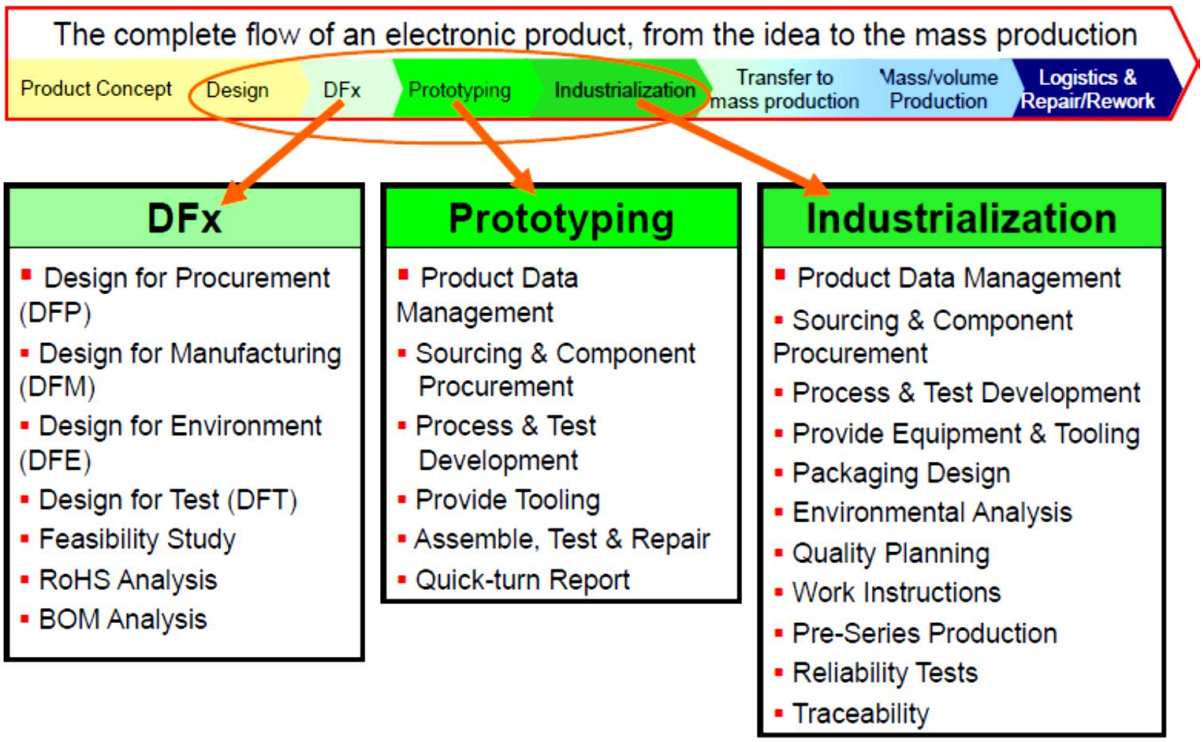


Figure 1.1: The complete flow of an electronic product – from the idea to the mass production (Source: Elect2eat 2007)

The quality of PCBs can be described by various characteristics, like existence of voids in the solder joints, existence of solder balls, wetting quality, stand-off, shear force, reliability, etc. These characteristics are influenced by a lot of factors, some of them being: materials (components, solder paste, stencil), layout of the board and of the stencil, production equipment, setup of the production equipment (for example, the temperature profile of soldering ovens) (Wohlrabe and Trodler 2012).

DFM has two primary components, DFF (Design For Fabrication) and DFA, being an essential concept today, in the global competition. DFM identifies various issues in the PCB structure and in the virtual prototype that can create manufacturing problems. Important to mention is that the DFM errors can manifest in some of the manufactured electronic modules/systems, while others will work correctly, this being the main difference between them and the DRC (Design Rules Check) errors, which affect all the manufactured electronic products.

Usually, the manufacturer disposes of specialized software tools in which the post-processing files received from the designer are loaded and checked, like the spelling checkers. The software generates a report containing the DFM issues/problems/errors, as follows: spokes on thermal reliefs (thermal pads) are too thin or too large, spacing violations, components conflicting, orientation issues, etc. Generally, this checking is done accordingly to IPC standards.

2 Virtual prototyping rules for DFM

The basic principles of DFM are the optimization, concurrent processes, changing the design process, use of intelligent CAD systems and other computer technologies, and knowledge of the production process from the conception (concept development) and design phases (Coombs and Holden 2016; Plotog and Vărzaru (n.d.)). Today, the high-performance design is based on eight fundamental concepts for optimizing the manufacturing processes.

1. Unit design

Unit design implies considering the electronic product as a whole that includes all subsystems and components, as well as all manufacturing, inspection, assembly and testing activities. If it is desired to improve some requirements, this must be done without adversely affecting the other requirements.

2. Simplification

The principle of simplification involves, first, simplifying the design of the system as much as possible, and then simplifying the design of the subsystems and the components of which they are composed.

Experience has shown that reducing the number of hole types on a printed circuit board reduces the number of drill types used in the manufacturing process, and thus fewer milling machine interruptions to replace them (Plotog and Vărzaru (n.d.)). This simplification example could be achieved without affecting the functionality of the respective module.

To simplify, it should be specified from the outset whether certain expected functionalities or features are absolutely necessary and what they are. Why? Because giving up certain functionalities or certain parameters leads to important simplifications in design, processing, and production, thus leading to a reduction in the selling price.

3. Minimization

Another basic principle of design for manufacturing is minimization. This is also the current trend in the electronics industry around the world. Among the advantages of minimization, it can be mentioned:

a. By reducing the variety on a printed circuit board, assembly time is also reduced because workers must perform fewer operations or movements.

b. By reducing the number of components to be produced, longer productivity periods can be ensured and time can be saved.

c. Each discarded component means lower costs for production, supply, transportation, storage, inspection, troubleshooting, maintenance, or reprocessing.

d. The smaller the number of components, the lower the complexity, cost, and effort.

4. Modularization

Modularization consists of dividing an assembly into subassemblies that can also operate separately, but which are connected to each other.

In the case of modularization of electronic assemblies, it is recommended to use the functional blocks already made together with other components, but only when:

- the operation of the resulting assembly is not affected;
- the requirements for facilitating repair & rework operations do not require that they be separated.

5. Standardization

Standardization can be defined as a specific activity through which are established, for real or potential problems, provisions intended for a common and repeated use, aiming to obtain an optimal degree of order in a given context (Anghelescu 2004). Another definition says that standardization is the action of standardizing, i.e. the organized technical regulation of production by specification, standardization, and unification to ensure product quality, material savings and increase labour productivity (Dexonline 2020).

ISO / IEC 2: 1996 defines the standard as a document, established by consensus and approved by a recognized body, which provides, for common and repeated use, rules, guidelines or characteristics for their activities or results, in order to obtain the optimal degree of order in a certain context (ISO - International Organization for Standardization) (ISO n.d.).

Standards vary in character, subject, or volume (ISO n.d.). These include several disciplines: starting with all the technical, economic, and social aspects of human activity and ending with all the basic disciplines such as language, mathematics, physics, etc.

- They are coherent and consistent: the standards are developed by the technical committees which are coordinated by a specialized body and ensure the overcoming of barriers between different fields of activity and different trade policies;
- Result from participation: the standards reflect the results of the joint activity involving all competent parties and are validated by consensus to represent all relevant interests: producers, users, laboratories, authorities, consumers, etc.
- There are active processes: standards are based on real experience and lead to material results in practice (products - both goods and services, test methods, etc.); they establish a compromise between the highest levels of progress and the economic constraints of time;
- They are updated: the standards are periodically revised or as the circumstances dictate in order to ensure their topicality and, therefore, evolve together with the social and technological progress;
- Have the status of references in commercial contracts and in court in case of a dispute;
- Have national or international recognition: standards are documents that are recognized as valid at national, regional or international level, as appropriate;
- Available to anyone: standards can be viewed and purchased without restriction.

As a general rule, standards are not mandatory, as they are voluntary. In some cases, implementation may be mandatory (such as in areas related to security, electrical installations, or public procurement). A standard represents a level of experience and technology that makes the presence of the industry in its development indispensable (Anghelescu 2004).

In the case of the electronics industry, in terms of design for manufacturing, it is recommended to standardize blocks, modules, subassemblies, manufacturing processes, systems whenever possible.

It is also recommended to use standard components from catalogues and to avoid old, technological obsolete components or the ones which are to be removed from production (Plotog and Vărzaru (n.d.)).

6. Design for easy inspection

The control and verification of the product during and at the end of the manufacturing process must be possible with as little time as possible, therefore the inspection must be as easy as possible.

For example, in the case of electronic modules, the components must be easily accessible and easy to identify. For this, the marking of the components on the PCB must be legible, ordered in one direction or at most two, and the components of the same type must have the same orientation. These are just a few rules to keep in mind when designing the electronic module.

7. Design for assembling

Design for Assembling (DFA) is part of the Design for Manufacturing and aims to make it easier to assemble any electronic product.

A DFA methodology involves two important issues (Coombs and Holden 2016; Plotog and Vărzaru (n.d.)):

a. to design with as few components as possible; this involves analysing the pairs of components to see if the two can be replaced with one;

b. to estimate the handling and assembly costs for each component using the appropriate assembly process.

In addition to reducing assembly costs, significant reductions in component costs are achieved, as well as improved reliability, reduced inventory, and production control costs.

8. Design for maintainability

Design for Maintainability is also part of the Design for Manufacturing and aims to establish benefits for both the manufacturer and the end user of the product. As the differences between the quality and price of products from different manufacturers are smaller and smaller, they will have to find new ways to attract customers, such as a higher degree of maintainability (Plotog and Vărzaru (n.d.)).

The argument for paying more attention to maintainability from an early design stage is that during the life of a product the maintenance costs are higher and higher.

As the cost of maintenance is an important factor in computing the total price of a product, it must be taken into account from the design phase, when the design flexibility is high and the costs of changing the project are low.

According to IPC-2222 standard, the manufacturing of electronic modules/systems can be of type 1 and type 2, as presented in figure 2.1. The virtual prototype is developed for performing various virtual investigations of the future product before manufacturing, in order to solve all the problems in the early stage of the development, for minimizing the design and manufacturing costs and shortening the time to market.

The A, B, C, X, Y, and Z classes offer details regarding the type and complexity of the electronic components used, as follows: A – through-hole devices (THD) only, B – surface mounted devices (SMD) only, C - simplistic THDs and SMDs intermixed assembly, X – complex

intermixed assembly, THDs, SMDs, and fine pitch BGAs, Y – complex intermixed assembly, THDs, SMDs, ultra-fine pitch components, chip scale, and Z – complex intermixed assembly, THDs, SMDs, ultra-fine pitch components, COB, flip chip, TAB.

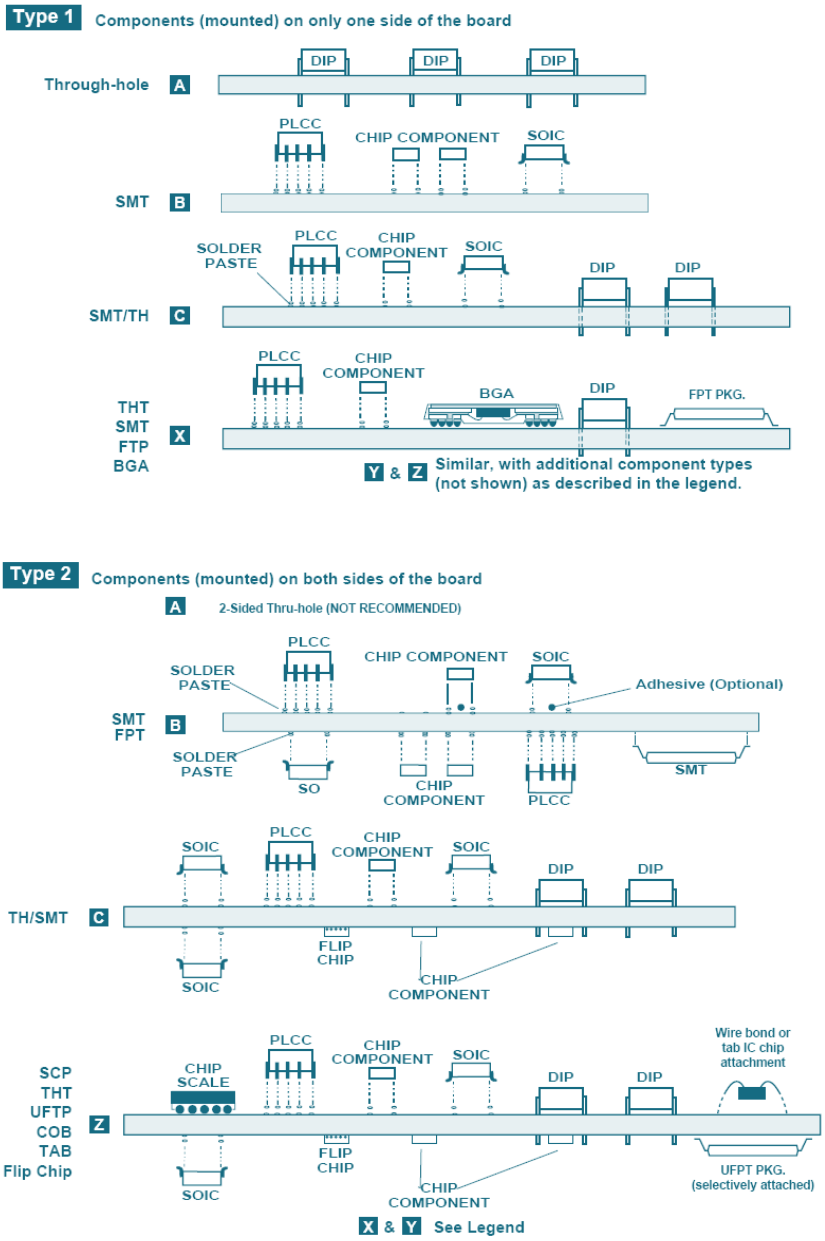


Figure 2.1: Assembling types according to IPC-2222 (Source: IPC 1998)

The virtual prototyping must support the design flow to satisfy the most important physical and technological requirements of the future real electronic module/system. Below are presented some of the most important DFM issues which must be considered as virtual prototyping rules when checking electronic projects (IPC 1998; IPC 2003).

1. Spacing of components

An important DFM issue is shown in figure 2.2, where it is presented the minimum spacing requirements imposed by the automated assembling which is performed in electronics factories.

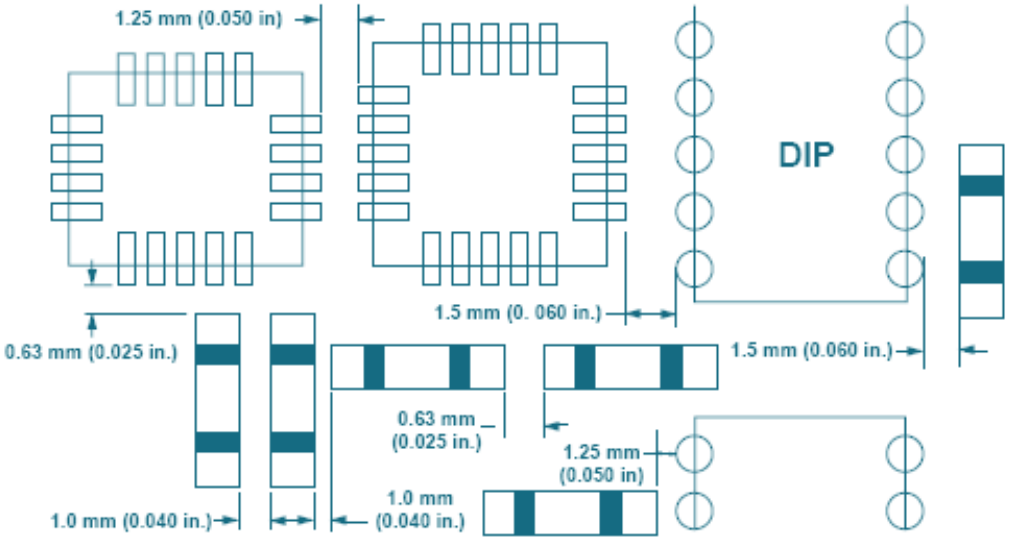
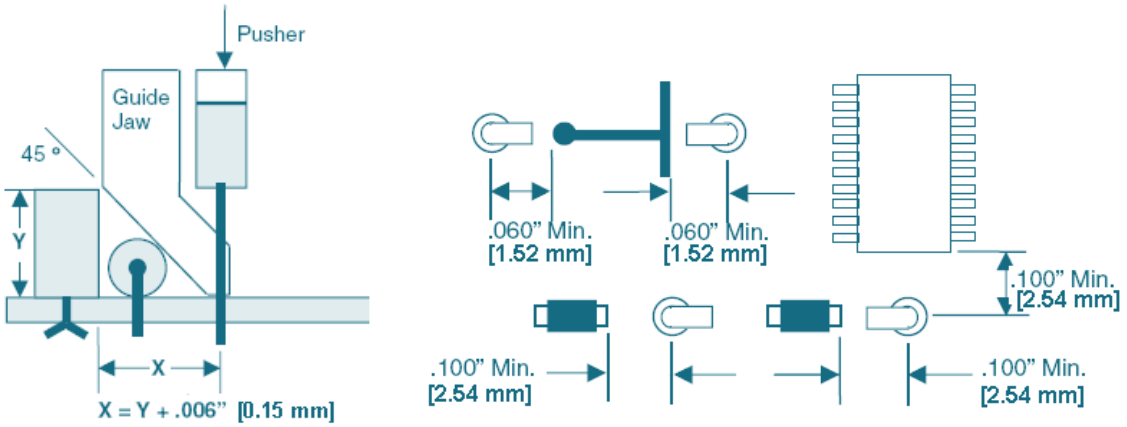


Figure 2.2: General spacing requirements according to IPC-2222 (Source: IPC 1998)

In the case of THDs assembling, the checking must be performed also for the height of the adjacent components (figure 2.3, a) and the bending or THD terminals on the opposite side, usually the BOTTOM side (figure 2.3, b).



a) b)

Figure 2.3: Spacing requirements of THDs according to IPC-2222 (Source: IPC 1998)

2. Fiducial markers (fiducials)

Fiducial markers (fiducials) are small conductive design items placed on the outer layers (sides) of the PCB. Fiducials are required if there are SMT components (SMDs) located on that side of the board and are used by the assembling equipment (pick-and-place machine) for location and alignment. The fiducial is, practically, a reference element that is observed by the vision system of the equipment and is required for a precise placement of solder-paste, adhesive, components, and for any other automated assembly operation. Without fiducials, the automated assembling process cannot be easily carried out (IPC 1998; IPC 2003).

Fiducials are classified as local fiducials (usually two, placed next to complex components, in diagonal), global fiducials (usually three, placed on the PCB), and panel fiducials (usually three, placed on the panel). Figure 2.4 presents their types and locations and figure 2.5 offers a zoom of the local fiducials associated to a complex BGA component/footprint.

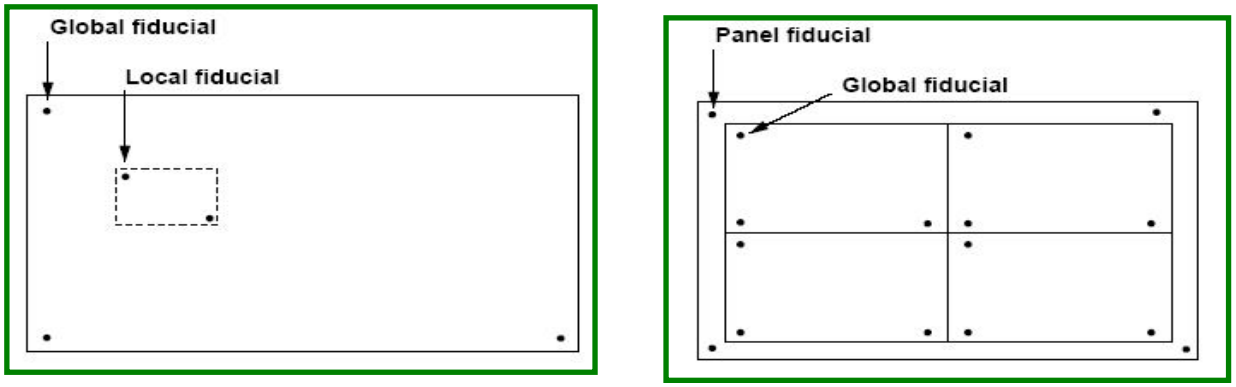


Figure 2.4: Fiducial markers (fiducials) – local, global, panel (Source: IPC 1998; IPC 2003)

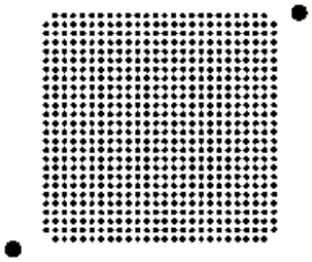


Figure 2.5: Detail of local fiducials placed next to a BGA component

Fiducials are allowed to have various shapes, according to figure 2.6, but the most used shape is the round one. An important DFM note is that the fiducial does not contain plated/non-plated hole.

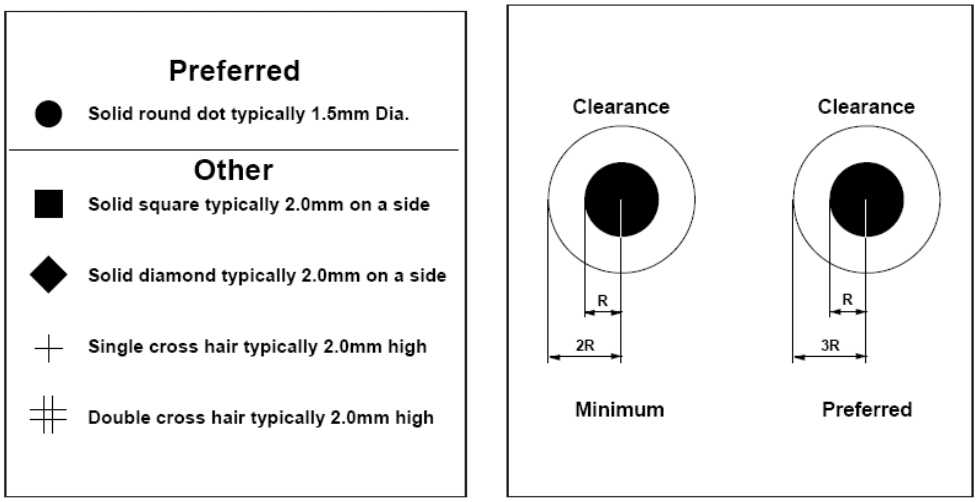


Figure 2.6: Shapes and DFM requirements for the fiducial marker

3. Thermal reliefs (TR)

Thermal reliefs (or “thermal ties”, “thermal pads”) are small conductive design objects, usually based on existing components’ pads/lands, which represent “wagon wheel” shaped pads

etched in the copper (figure 2.7) of a signal or power & ground layer around the pads which must be connected to large copper areas (planes). TR realizes a connection through two or more narrow tracks (called bridges, spokes or webs) across an opening in the plane, avoiding the direct connection to the plane for minimizing the heat transfer to the plane by conduction and allowing a high-quality soldering (IPC 1998; IPC 2003). Multi-layer PCBs with inner power and ground planes connected to plated through-holes (used for THDs) require TRs also on those inner planes. This is because the copper planes act as heat sinks for components pins/pads during the soldering process, the area not reaching the required temperature for a good solder joint. Thermal reliefs maintain the electrical connectivity, but restrict the heat sinking effect. Additionally, if SMDs must be soldered to bigger pads or partial planes, TR structures must be introduced in the layout for a proper soldering (Coombs and Holden 2016).

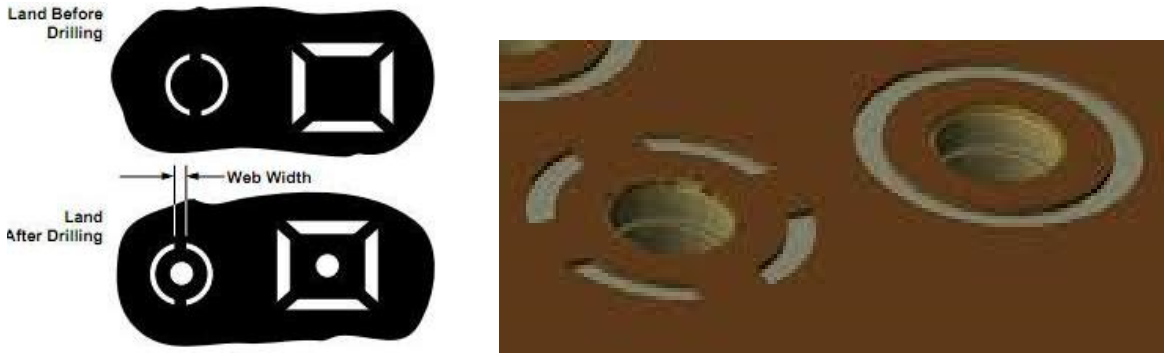
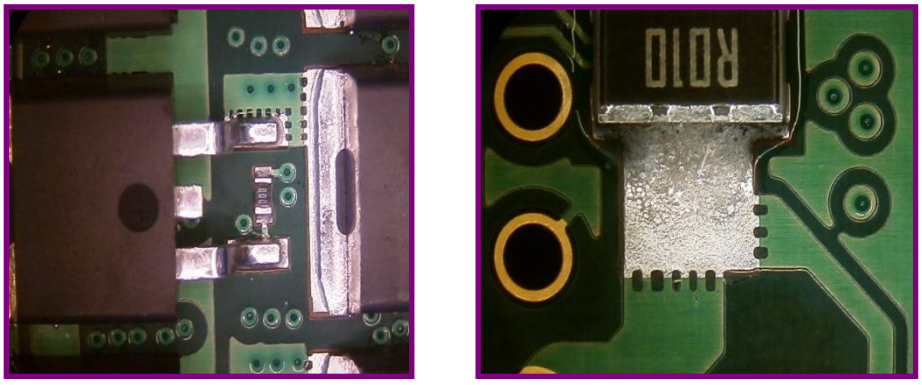
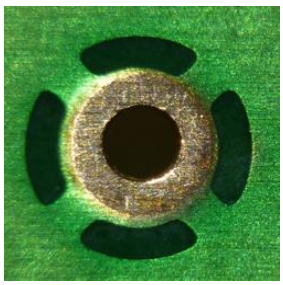


Figure 2.7: Thermal reliefs (TR) according to IPC-2222 (left) and a 3D general view of the TR in relationship with a pad non-connected to the plane (right)

The thermal relief acts as a thermal decoupling item, creating a weak thermal conduction in dynamic regime (during soldering), but it allows a quite good thermal conduction in static regime (during the working of the module/system)



a)



b)

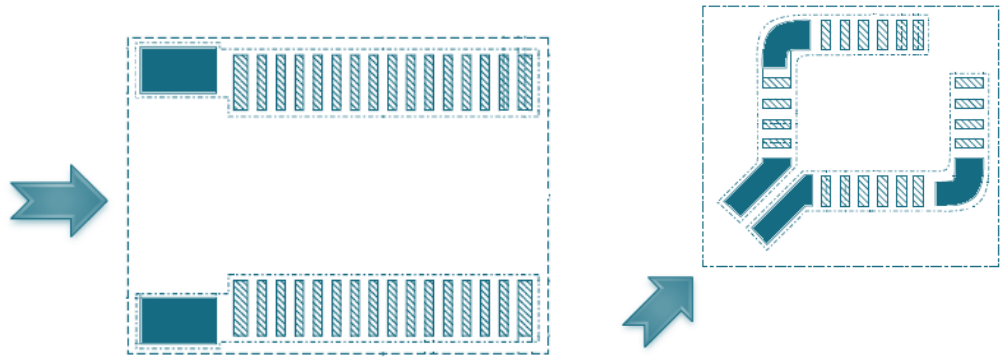
Figure 2.8: Thermal reliefs (TR) in real electronic modules/systems (a) and a zoom of a real TR (b)

IPC-2222 accepts a minimum of 2 bridges/spokes for a proper connection of the TR to the plane, but 4 bridges are recommended. The total width of the pad-plane contact must be minimum 60% of the minimum dimensions of the pad, calculated as: maximum diameter of the hole + 2 x conductive annular ring (width) + tolerance. The total width of the contact is equal with the product of the width of the bridge and the number of the bridges.

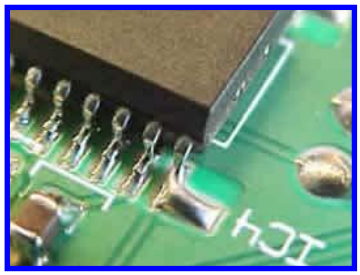
4. Solder thieves (ST) in case of wave soldering

Solder thieves (ST) are small conductive design items placed on the outer layers (sides) of the PCB for preventing solder bridging during the wave soldering process (figure 2.9). Sizes of the solder thieves on the PCB must be large enough to form an enough traction force during wave soldering, so the molten solder alloy will not leave these special pads, therefore it will not cause short circuits by bridging in the printed circuit (Coombs and Holden 2016).

In some cases, wave soldering components below 1.25 mm (50 mil) pitch should be avoided and questioned during design for manufacturing (DFM) reviews of the electronic project, since it takes more effort from the equipment and process engineers. Soldering 0.8 mm (32 mil) pitch can be achieved, 0.6 mm pitch is problematic and 0.5 mm pitch or less on the PCB requires more rework activity.



a)



b)

Figure 2.9: Solder thieves (ST) created in PCB footprints (a) and a zoom of a real ST in the frame of an electronic module (b)

SOIC and QFP components benefit from solder thieves on the trailing edge of the packages, but only if the solder shorts are on the last pins. The solder thief pad must always be a minimum of three times the length of the last pad and on the same pitch. When using QFPs, the component is positioned at 45° to the direction of travel through the wave (figure 2.9 a), imagine from right). The solder thief takes the additional solder alloy during the wave soldering, avoiding the short-circuits created by bridging. As observed in figure 2.9 a), imagine from right, additional STs must be properly placed in other corners, according to the direction of the board in the oven and in relationship with the specific wave of the molten solder alloy created by the oven.

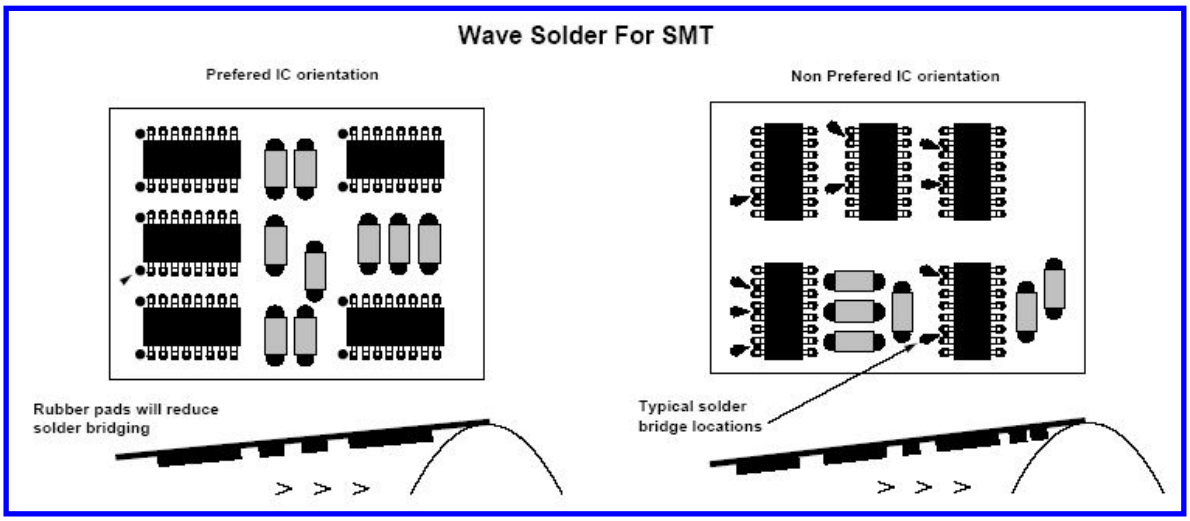
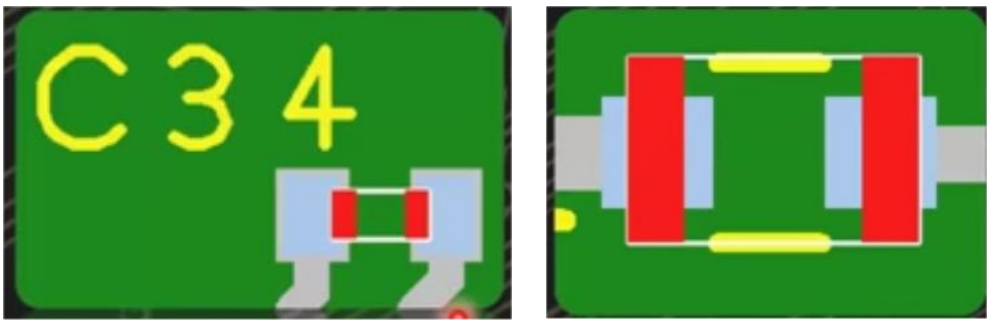


Figure 2.10: Solder thieves (ST) and preferred/non-preferred orientation of integrated circuits during wave soldering

5. PCB footprint – real electronic component mismatch

The mismatch between the PCB footprint/pattern allocated by the designer and the real electronic component which must be placed on the printed circuit board during the assembling process is an important DFM issue because it can create important problems during the assembling, but also during the whole lifetime of the electronic product (Biggs 2018).

Figure 2.11 a) presents a small component placed on a big PCB footprint (0402 chip component placed on a 0603 PCB footprint) and figure 2.11 b) presents a big component placed on a small PCB footprint (0805 chip component placed on a 0603 PCB footprint).



a) b)

Figure 2.11: a) 0402 chip component placed on a 0603 PCB footprint; b) 0805 chip component placed on a 0603 PCB footprint

In many cases, the errors are caused by the confusion between the code of the component in Metric and in Imperial systems of units. For example, for chip components, the component coded 0603 in Imperial is coded 1608 in Metric and the component coded 0603 in Metric is coded 0201 in Imperial (see figure 2.12).

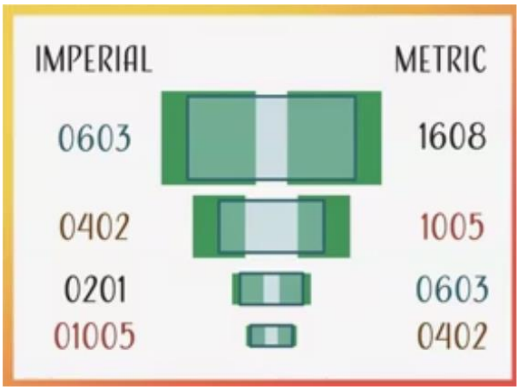


Figure 2.12: Codes of chip components in Imperial and in Metric systems of units

Figure 2.13 shows another type of PCB footprint – real component size mismatch. The component is not the same size as the footprint (it is smaller), although the aspect of the package looks similar. Very likely, there is a wrong footprint attached to a component part number. Additionally, errors can appear due to the mismatch between SMDs and THDs.

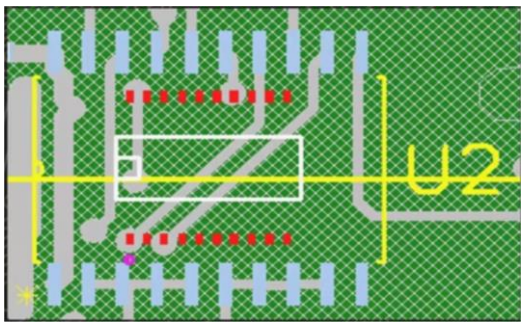


Figure 2.13: The component is not the same size as the PCB footprint for the U2 SMD integrated circuit

Another DFM issue related to this topic is named “polarity issue” and represents the wrong allocation of PCB footprints/patterns to polarized electronic components, such as: electrolytic capacitors, various types of diodes and transistors/thyristors, potentiometers/trimmers, connectors, and other special components with restricted placement and orientation. One special issue is when the footprint is correct, but the polarity indicator is missing, especially for electrolytic capacitors and diodes. Due to a poor design, polarity markings are not very clear to interpret on the PCB footprint or are totally missing (figure 2.14), which can create major problems during the assembling stage of the electronic module/system.

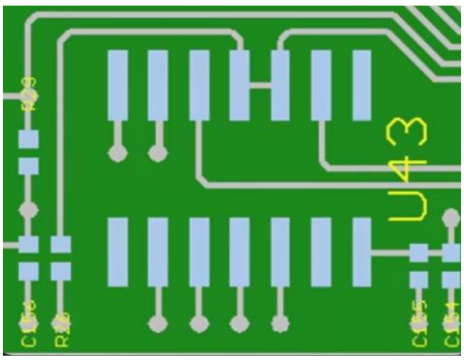


Figure 2.14: Pin 1 indicator for the U43 SMD integrated circuit is missing

Related to “Pin 1 indicator”, in case of DIP components, DFM specifies that the PCB footprint must be designed with circular pads, with one exception, the first pad. Pin/pad 1 must have a square shape in order to clearly indicate the orientation of the component without the help of the silk screen. Figure 2.15 presents this DFM issue existing on the IFRO test board.

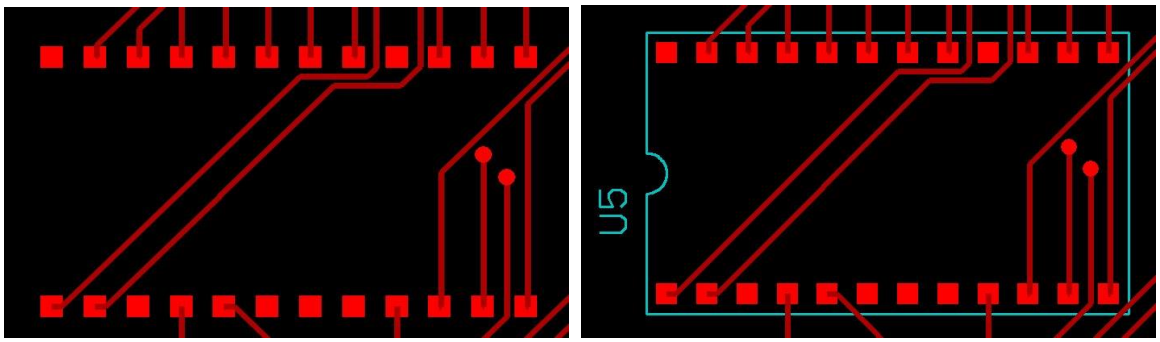


Figure 2.15: Pin 1 indicator for the U5 THD DIP package is missing on the electrical layer, the package orientation being indicated only on the silk screen non-electrical layer

6. Undefined or very small electrical and non-electrical line widths

During the PCB design stage, the designer can wrongly define or can totally leave undefined some electrical and non-electrical lines of the virtual printed circuit board and future electronic module/system. These narrow lines, without a proper CAM optimization performed by the PCB factory, will be impossible to be manufactured or will be produced with errors. Figures 2.16 and 2.17 show such an issue on the IFRO test board, developed before the DFM checking and optimization were performed.

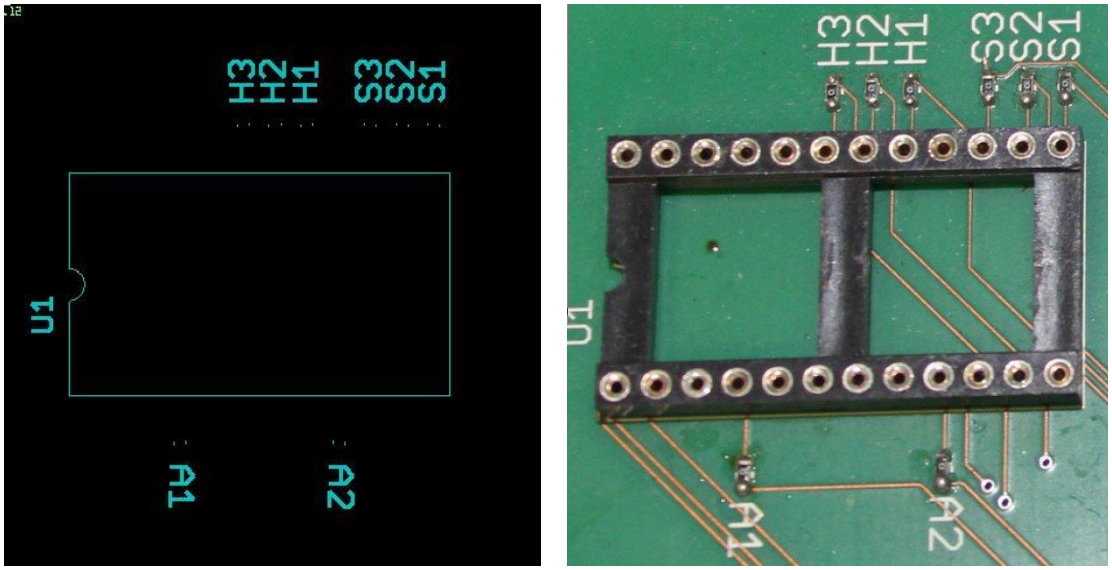
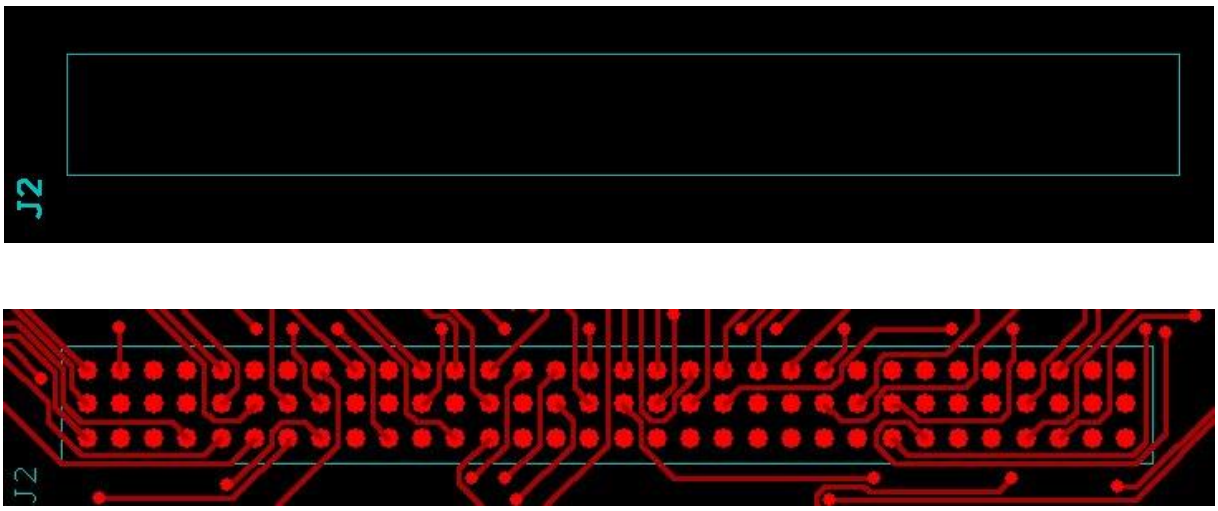


Figure 2.16: The outline of U1 and the marks of SMDs on silk screen were defined with too narrow lines in the PCB design process

In figure 2.16, the U1 DIP package (socket) and A1, A2, H1, H2, H3, S1, S2, S3 SMD chip components can be observed in both virtual and real stages. The outline of U1 and the marks of SMDs on silk screen were defined with too narrow lines (0.13 mm, see in figure 2.18 the details for D24 aperture/D-code based on a CAM tool) and the PCB producer was obliged to increase the width of the ink lines to approx. 0.2 mm in order to be able to manufacture correctly the test board.



b)

Figure 2.17: The J2 connector outline was defined with a too narrow line, difficult to be manufactured

The same DFM issue can be observed in figure 2.17 for the J2 connector outline.

Figure 2.18 presents also info for D23 and D25 apertures, of 0.18 mm and 0.15 mm, highlighting that both are at the manufacturability limit. The problems can be solved if the designer receives from the PCB factory the equipment and processes limits in the early design stage, in order to know from the beginning the boundaries of the virtual prototype development.

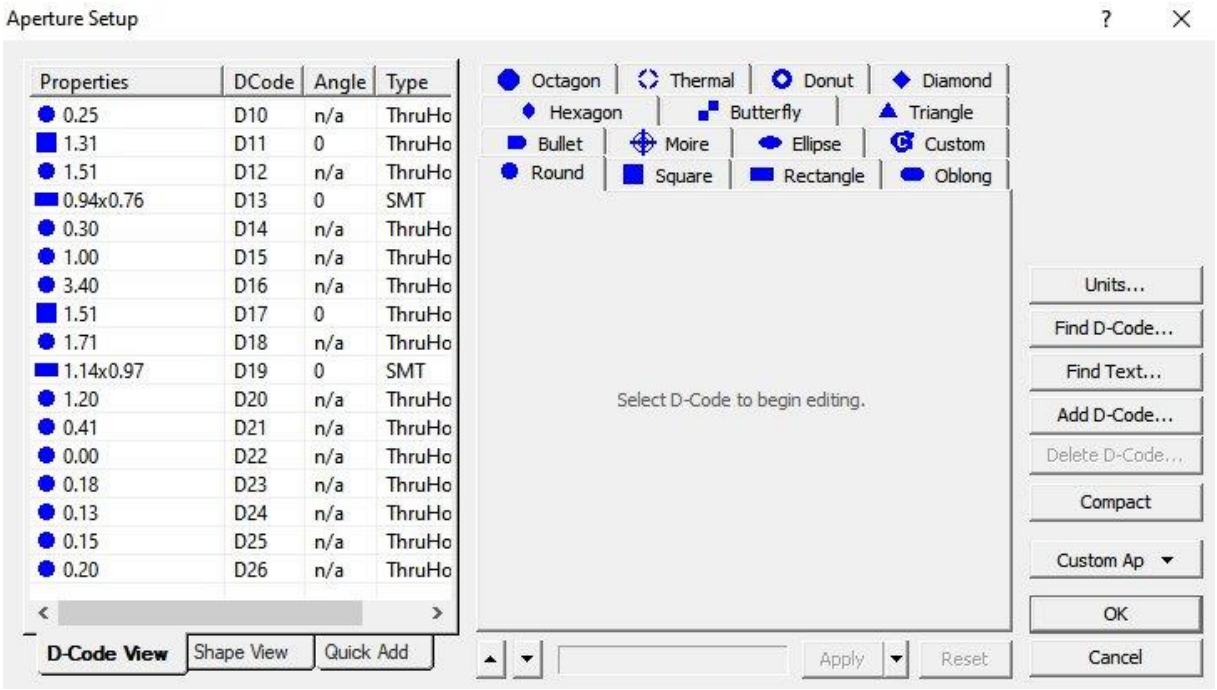


Figure 2.18: A CAM tool indicates the narrow lines (D24 aperture/D-code, for example) of the PCB project, which is a DFM issue and can create manufacturing problems

The best solution for solving the undefined electrical and non-electrical lines is to have a CAD tool that increases automatically these lines to a specific and safe value, as presented in figure 2.19 in the case of Cadence OrCAD PCB Editor design system. In the right side, there is a special

box named “Undefined line width” where the designer can specify a minimum manufacturable value for any undefined line.

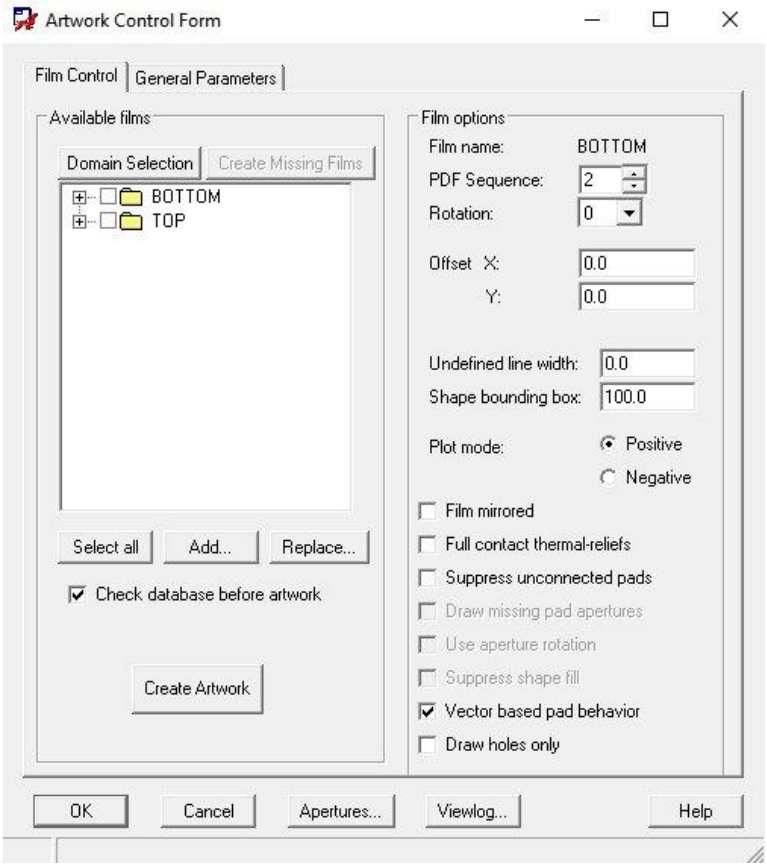


Figure 2.19: A CAD tool panel which solves the problem of undefined lines

For optimizing the thermal management of the IFRO test board based on DFM concepts, it will be necessary to re-design it based on PCB thermal design considerations, the key elements being the thermal spreading planes and the thermal vias for mitigating the dissipation demands of the CERDIP24 packages in the early stage of the PCB design.

In the case of CERDIP24, the most important parameters are the junction temperature of the package, the top temperature, the case temperature (the temperature of the highly thermally conductive pads of the package and the attached PCB), the ambient temperature and the thermal resistances between these “thermal nodes” (figure 2.20).

The goal of UPB for the future re-design stage will be to create the lowest thermal resistance possible between the semiconductor junction and the ambient environment. Except for θ_{CA}, the thermal resistances of the system (θ_{JT}, θ_{TA} and θ_{JC}) are defined by the properties of the package and can be taken from the datasheet. UPB will act on and optimize the value of θ_{CA}, which is dependent on the PCB design.

The challenge will be the increasing of the thermal transfer between the CERDIP24 case and the ambient environment by reducing this resistance, for minimizing, finally, the thermal resistance between the junction and ambient environment.

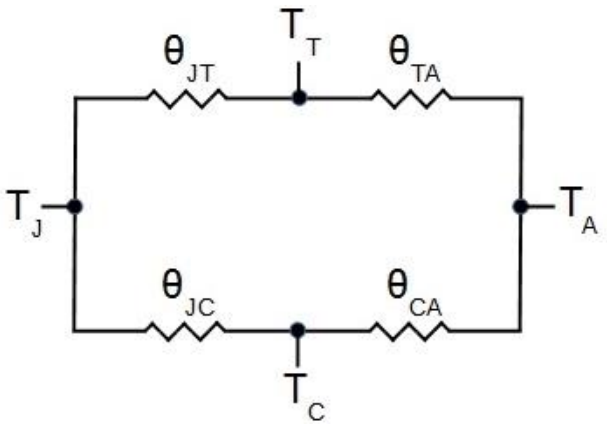


Figure 2.20: Thermal resistances between the "thermal nodes" of the CERDIP24 package

The approach for the heat transfer is based on thermally connecting the packages to the thermal spreading planes which will be developed during the re-design, directly or with the support of thermal vias. These vias will provide a thermal conduction path to the copper plane created on the bottom side, additionally to the plane generated on the top side of the test board.

The thermal resistance of a thermal via, θ_{TV}, can be calculated with the formula found in (Coombs and Holden 2016) and is usually in the range of 20 - 80 K/W. Since the thermal resistance is analogous to the electrical resistance, an array of 4 x 4 thermal vias placed under the package, in total of 16, will have a thermal resistance of $\theta_{TV}/16$ because all the 16 thermal vias are connected in parallel, thus increasing the thermal performance.

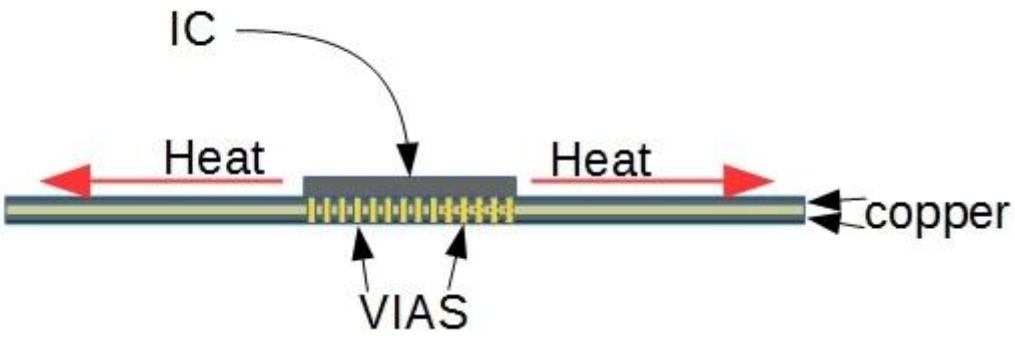


Figure 2.21: Heat transfer by conduction based on thermal spreading planes and thermal vias (Source: Coombs and Holden 2016)

The two copper planes on top and bottom sides of the PCB will be properly connected with thermal vias for increasing the efficiency of thermal dissipation at the PCB level. If necessary, a 4-layer design will be considered because such a structure can increase the dissipation capacity of the PCB up to 30%, when comparing the same area of a 2-layer design. Generally, the following DFM thermal design rules will be taken into account:

a. In order to dissipate 1 W, the board needs to have a copper area of 15.3 cm² for a 40°C rise in board temperature, assuming that the package is thermally coupled to the copper plane that extends to the edges of the board and that the board is positioned so that air can flow freely around both sides of PCB.

b. Because the IFRO test board has 8 CERDIP24 placed on a board area, UPB will analyse to place those components in such a way that the PCB will be evenly heated by these components, if all will be powered. Big temperature differences across the board area do not allow the PCB to optimally transfer the thermal energy away and will create hotspots. Because UPB has a good expertise in thermal imaging, thermovision/thermography will be used for obtaining the thermal map/pattern of the actual test board, in order to optimize the second release of the test board.

c. The more thermal vias placed below the package, the better the PCB will transfer the thermal energy to the copper planes. For each package, the thermal vias will be configurated in array to increase the thermal transfer by conduction.

d. UPB will use a thickness of 105µm or more for the copper on top and bottom sides of the test board for increasing the quality of the copper planes heatsinks.

e. In the case of the thermal spreading planes, it will be important that the plane to be not interrupted by PCB traces routed perpendicular to the thermal path and cutting the copper heatsink.

The DFM rules from above and the more advanced thermal design techniques which will be used during the PCB design process, will allow UPB to have a better control of the temperature on the IFRO test board after the re-design stage and will optimize the thermal map/pattern during the functioning.

3 Principles of PCB footprints design for DFM

When the design of a new footprint is necessary, the designer has access to component datasheets but also to the JEDEC standards (drawings) regarding the component packages. These offer various information about the package dimensions, but do not usually offer information about the pads dimensions and positions (PCB land pattern). These last ones are determined also by the assembly technology (IPC 2005; IPC 1996).

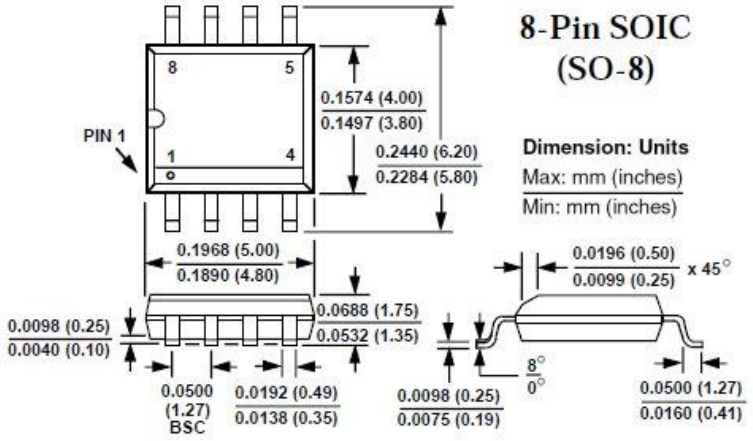
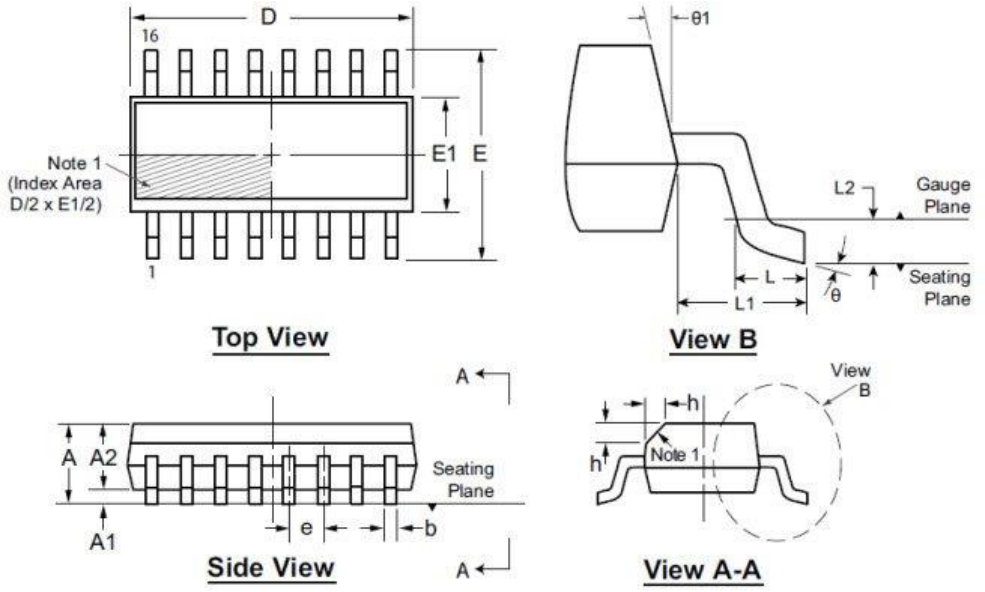


Figure 3.1: Package dimensions from a manufacturer datasheet



Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

Figure 3.2: JEDEC SO package symbol naming conventions and typical dimensions (MS-012AA)

IPC standards, on the other side, provide information on pad sizes, based on terminal sizes. Usually IPC standards give the distances to the edges of the pads, requiring a transformation calculation because in CAD programs, when designing the footprint, the size of the pads and the distances between their centres must be known. So, some calculation is required to

convert the tables from IPC to the corresponding footprint in CAD programs, as OrCAD PCB Editor.

In conclusion, the design process of a package involves the transposition in CAD programs of the information regarding a certain package from the JEDEC standard, simultaneously having in mind the recommendations from the IPC standards (IPC 1996).

Based on the information in Fig. 3.1 and/or Fig. 3.2, the designer must be able to determine the length of the pads Wp and the width of the pads Hp, or briefly the padstack, as the preferred term used in CAD programs. In addition, the distances between the pads in the OX and OY directions, SE and Se, must be determined, according to figure 3.3a (Mitzner 2009).

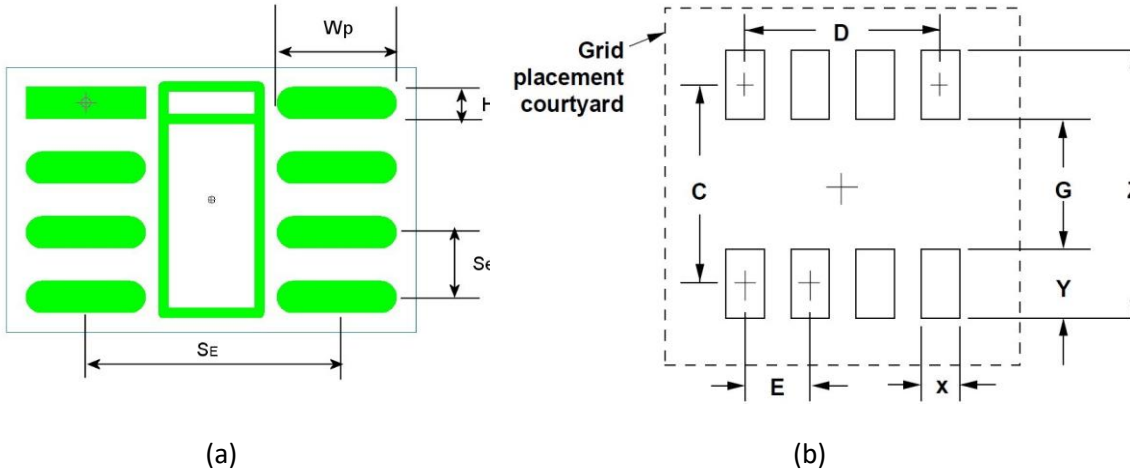


Figure 3.3: a) Package footprint in a CAD program, b) Symbols for different dimensions used in IPC standards

In Fig. 3.3b, it can be seen how the recommendations from IPC standards are given, mostly as distances between the pads or between the edges of the pads.

The size of a well-chosen SMD pad ensures a quality solder joint between the component terminal and the PCB. The size of the pad must be chosen to take into account certain variations in the size of the component, the manufacturing tolerances of the PCB, the tolerances of the placement process but also the specifications on the shape of the solder, the meniscus or solder fillet.

THT components have larger dimensions and therefore the choice of their pads is less influenced by these tolerances, in contrast to SMD components which are usually much smaller and for which there is an increased sensitivity to manufacturing tolerances regarding the choice of pads. The IPC-7351 standard (which replaces the IPC-SM-780/2) is the standard used to design the SMD component footprints of both the padstack and the full footprint.

The geometry of an SMD solder joint according to IPC standards is shown in Fig. 3.4.

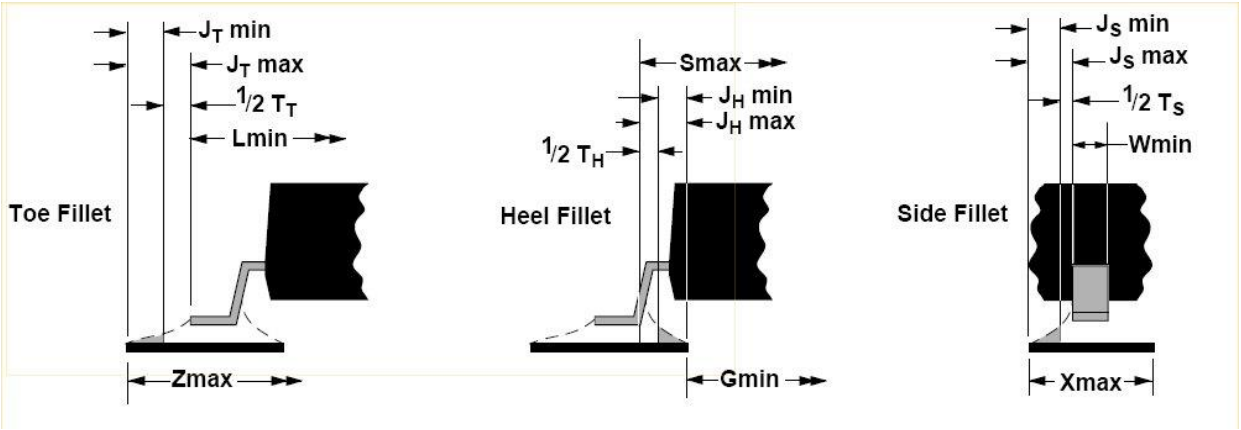


Figure 3.4: Solder joint geometry and the characteristic dimensions (Source: IPC 2005)

The solder pad must be, in general, larger than the terminal to allow proper soldering. It was used the JT notation for the distance from the edge of the pad to the tip of the terminal (Toe). JH is the distance from the edge of the pad to the heel of the terminal (Heel) and JS is the distance from the sides of the pads to the side edges of the terminal (Side).

The values of JT, JH, and JS depend on the type of component and the desired density level (A, B or C). Density level is a different type of level than the productivity level in IPC standards.

For the normal density level, these values are given in the following tables, according to the IPC-7351 standard (pp. 8 -14).

Package type	Mils	Millimetres
Gull wing (SOG)	14	0.35
J lead (SOJ)	14	0.35
Chip Components (0603 and larger)	14	0.35
Chip Components (smaller than 0603)	4	0.10
Small outline (SO)	12	0.30
Tantalum capacitors	6	0.15
Leadless Chip Carrier (LCC)	22	0.55
MELF	16	0.40

Table 3.1: The value of the JT parameter for different components

Package type	Mils	Millimetres
Gull wing (SOG)	14	0.35
J lead (SOJ)	-8	-0.20
Chip Components (all)	-2	-0.05
Small outline (SO)	0	0.00
Tantalum capacitors	20	0.50
Leadless Chip Carrier (LCC)	6	0.15
MELF	4	0.10

Table 3.2: The value of the JH parameter for different components

Package type	Mils	Millimetres
Gull wing (SOG) (pitch higher than 0.625mm)	1	0.03
J lead (SOJ)	1	0.03
Gull wing (SOG) (pitch smaller than 0.625mm)	-1	-0.02
Chip Components (0603 and larger)	0	0.00
Chip Components (smaller than 0603)	0	0.00
MELF	2	0.05
Small Outline (SO)	-2	-0.04
Tantalum capacitors	-2	-0.05
Leadless Chip Carrier (LCC)	-2	-0.05

Table 3.3: The value of the JS parameter for different components

In order to design the footprint in CAD programs, it is necessary to find out the width of the pad, *WP*, and the height of the pad, *HP*, according to the following relationships:

$$W_{\mathrm{P(MAX)}} = E_{\mathrm{MIN}} - (E_{\mathrm{MAX}} - 2L_{\mathrm{MIN}}) + 2J_{\mathrm{T}} + 2J_{\mathrm{H}} + 2\sqrt{(E_{\mathrm{TOL}(\Delta)})^2 + F^2 + P^2}, \quad (3.1)$$

$$H_{\mathrm{P(max)}} = b_{\mathrm{MIN}} + 2J_{\mathrm{S}} + \sqrt{(b_{\mathrm{TOL}(\Delta)})^2 + F^2 + P^2}, \quad (3.2)$$

E (MIN and MAX) are distances between the terminal edges according JEDEC in Fig. 3.2; *E*TOL(Δ) is the tolerance of *E* equal to (*E*MAX -*E*MIN);

L is the terminal length to be soldered to the pad;

F is the PCB manufacturing tolerance: 0.1mm (4 mils) typical;

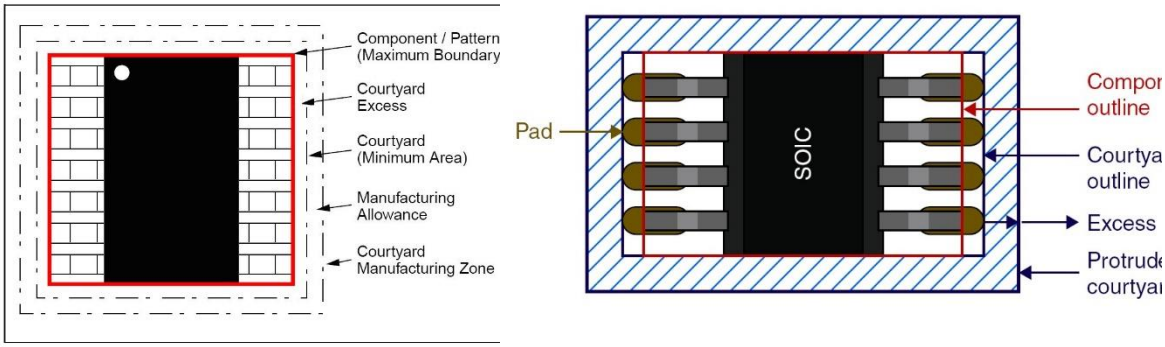
P is the placement tolerance of the pick-and-place machine: 0.15mm (6 mils) typical;

*b*MIN is the minimum width of the terminals, bTOL(Δ) is the tolerance of *b*= (*b*MAX - *b*MIN);

*J*T şi *J*H and *JS* are chosen from IPC-7351 standard, *J*T =0.3mm (12mils), *J*H=0, *JS*= - 0.05mm (2mil).

SMD Footprint (Package Symbol) Design

After designing the pads, they must be placed properly to complete the correct footprint. The specific arrangement of the pads (land pattern) according to the IPC-7351 standard is shown in figure 3.5 for a SOIC circuit (IPC 2005).



(a) (b)

Figure 3.5: Defining the contours associated with a package according to the IPC standard (a) and in a CAD software package (b); Component outline, Overall contour - courtyard, Excess outline - Protruded courtyard (Source: Mitzner 2009)

The outline of the component - component outline defines the external dimensions of the integrated circuit, being its maximum external border that includes both the limits of the package body and of the terminals.

Then, another contour is defined as "courtyard" - courtyard around the component, an outline that includes the body and solder pads. This contour is further adjusted to the outside of the component, so that the contour enters (protrude) into the area intended for other PCB articles, consuming from the reserved area, for example for routes.

The value of the protrusion called the courtyard excess will determine the minimum spacing between the components during placement operations. A large value of this excess distance makes the placement density of the resulting board to be lower.

There should be carefully seen how different software packages are using this implementation in realizing the footprints. For instance, the OrCAD PCB Editor system does not use the concept of courtyard as defined by the IPC-7351 standard. Figure 3.6 shows a SOIC8 package showing the Place boundary outline in PCB Editor over which was drawn the “courtyard” contour that “protrudes” the outside according to IPC standard.

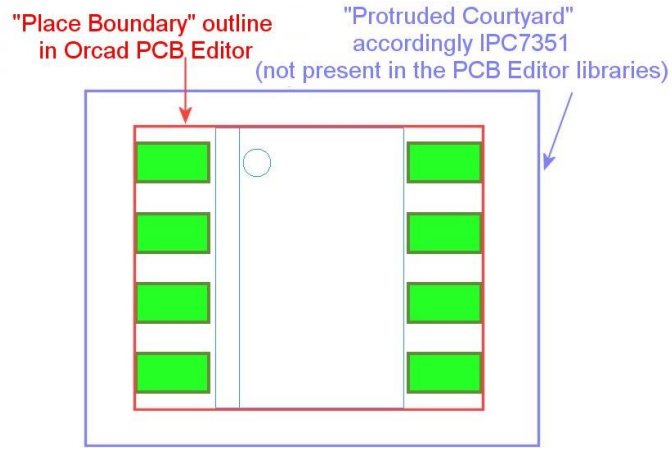


Figure 3.6: The outlines of a component in the PCB Editor system

Note that in PCB Editor the Place Boundary outline does not include excess space at the ends of the component body or around the terminals. For most packages, in the original PCB Editor library, the excess space is non-existent. In the program settings of the Constraint Manager utility, the designer cannot introduce the package spacing, being also the case of the OrCAD Layout suite. Electrical Rule Checks (ERC) report errors only at the intersection of Place Outline contours. To obtain the desired placement densities, it is necessary to change the footprints or to choose an appropriate, larger placement grid, and then visually check the placement individually.

Another example of how package outlines are treated is shown in figure 3.7, being the case of the software OrCAD Layout.

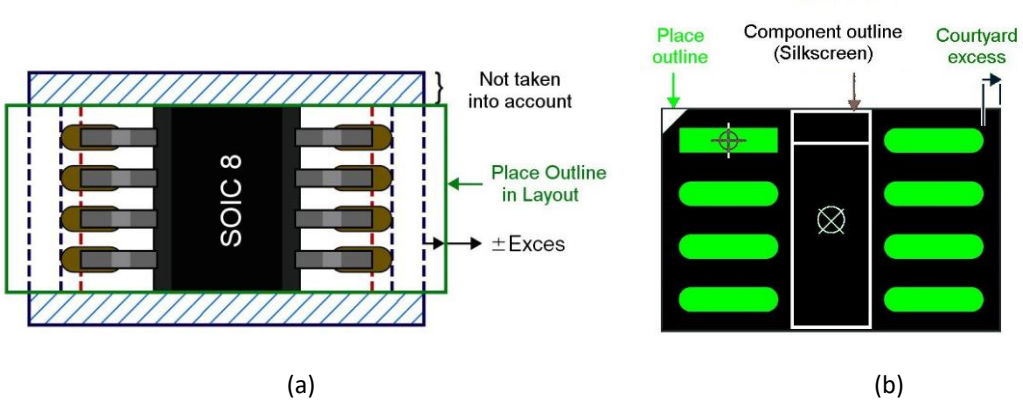
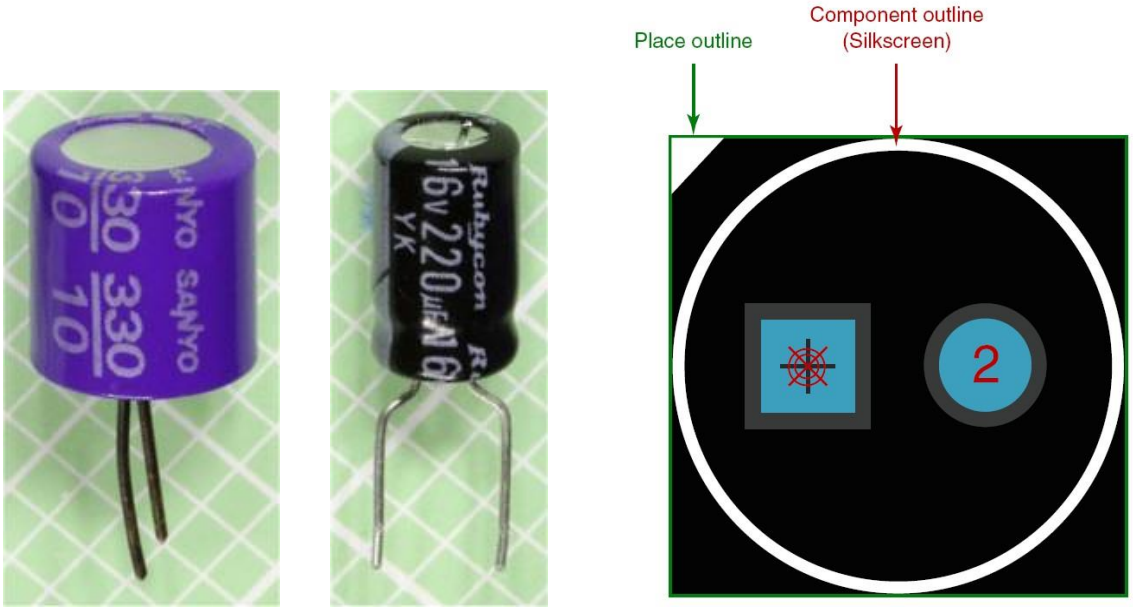


Figure 3.7: a) Components outlines in Orcad Layout, a) Courtyard excess only in X direction, b) aspect of the footprint (Source: Mitzner 2009)

Design of the footprint for THT packages

a) Radial THT components

An example of an electrolytic capacitor with radially arranged terminals is shown in the figure 3.8.



(a) (b) (c)

Figure 3.8: Electrolytic capacitors with radial terminals a) without preforming, b) with preforming c) footprint elements in CAD programs

For this type of components, the structure of the footprint results directly from the construction of the component. The distance between the pads is equal either to the distance from where the terminals protrude from the component body or to a predetermined distance in the case of components with preformed terminals.

b) THT axial components

Example for a typical carbon film resistor.

Determining the distance between pads

The design of the footprint for axial components is much more diverse than that of radial components. The standard IPC-CM-770, Sections 11.1.8, p. 67, as well as other sources in the literature, provide general rules for footprint design (IPC 1996).

According to IPC-CM-770 standard, the lead should extend approximately one diameter of the lead out of the component body. This distance to the radius of curvature is either expressed as "lead diameters" or is at least 0.8 mm (32 mil). The end of the body of the component is so defined as to include any meniscus of the protective coating, sealing with solder alloy, weld bead or any other extension.

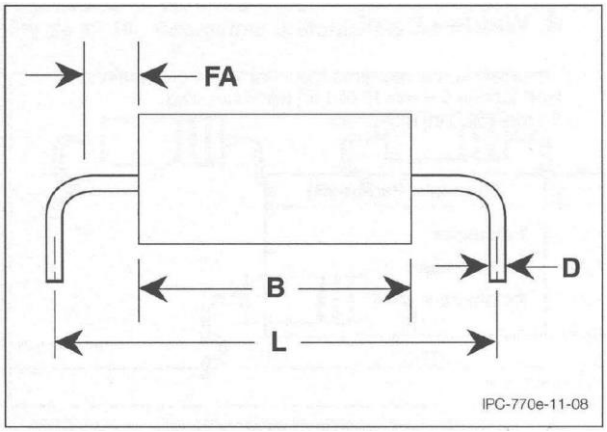


Figure 3.9: Bend configuration for through hole components

In figure 3.9, one can visualize the elements used to compute the minimum distance centre to centre lead spacing. This can be calculated with the following equation:

$$C/C = B_{\max} + 3 \times D^{*} + 2 \times FA \tag{3.3}$$

where:

C/C = centre to centre lead spacing;

B = length of the component body;

D = nominal lead diameter;

FA = space required to form the lead (forming allowance), lead should not be disturbed within this distance; *FA* = *D* or 0.8 mm, whichever is higher.

* For lead diameters up to 0.8 mm the factor is 3×*D*. The factor is 4×*D* for lead diameters between 0.8 mm and 1.2 mm and 5×*D* for lead diameters over 1.2 mm.

The value of "*C/C*" is usually adjusted upward to coincide with the grid used. The total length of both leads should not exceed 25 mm in length unless this component is mechanically supported to the printed circuit board.

It was applied the calculation mode based on the IPC standard, with the notations from figure 3.10. The position of the padstacks depends on the length of the component body, but also on the bending place of the terminals, i.e. on their preforming.

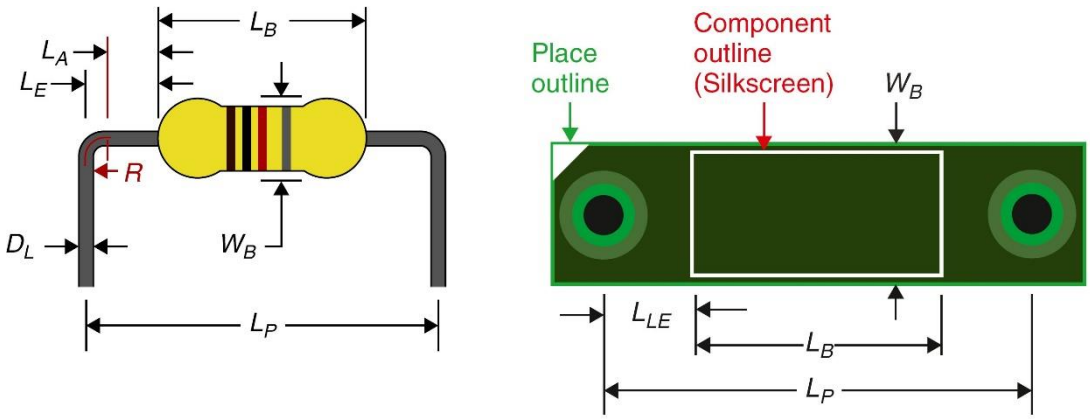


Figure 3.10: Component with axial terminals b) Elements of the footprint (Source: Mitzner 2009)

The minimum distance between the pads is calculated with the relation (3.4):

$$L_P = L_B + 2(R + L_A) \tag{3.4}$$

with L_P the distance between the pads, L_B the length of the component body, R the allowable bending radius, according to Table 3.4, L_A the length of the terminal extension from the body to the beginning of the curved portion (minimum distance from the body from which the terminals can be bent), L_A will also be taken from Table 3.4. L_E is equal to the sum between L_A and R.

D_L (mils)	R (mils/mm)	L_A (mils/mm)
$D_L < 31$ (0,8mm)	$1{,}0 \times D_L$	31 (0,8mm)
$31 \leq D_L \leq 47$	$1{,}5 \times D_L$	D_L
$D_L > 47$ (1,2mm)	$2{,}0 \times D_L$	D_L

Table 3.4: Permitted values of the bending radius and distance from the component body

It is observed from Table 3.4 that both R and L_A depend on the diameter of the lead D_L.

Once the minimum distance has been calculated, the pads are placed at the nearest distance in the standard working grid. Most of the time, a one-module or 100 mil grid is used, but if this value is too high, a 25 mil grid is usually chosen. Finally, it is necessary to check the total length of both terminals, which must not exceed 1 inch (25.4 mm) without additional mechanical support for the component, as specified above.

Hole to lead ratio

The size of the plated through-hole (PTH) must be large enough so that the terminal can easily protrude through the hole, but it must not be too large so that the capillarity phenomenon during soldering does not occur properly. Two methods can be used to determine the

diameter of the hole depending on the diameter of the lead, one based on a calculation and another based on the existence of a pre-calculated table.

The first method is derived from the IPC-2221A standard, Section 9.1.3, p. 74 and C. Coombs ed. 5, Section 42.2.1, p. 42.3. This method takes into account the thickness of the hole metallization (assumed or known) and allows the user to define a tolerance factor *k*. The method results in obtaining values of the space between the terminal and the metallized hole (clearance) which depends on the diameter of the lead.

The diameter of the drill bit is given by the relation (3.5).

$$D_H = (D_L + 2T_P) \times k \tag{3.5}$$

with D_L the diameter of the lead, T_P the thickness of the metallization in the hole (if no data is available, take T_P = 1 mil), and *k* is a user-defined tolerance factor, 1.05 < *k* < 3.0 (recommended value of 1.5).

It has been found that the previous relation gives too large dimensions of the free space in case of large diameters of the terminals and needs to be corrected. The diameter from which this correction is to be applied is not specified in the literature.

For example, if the lead diameter of a component (D_L) is 0.9mm (36 mil), then the diameter of the hole must be (Mitzner 2009):

$$D_H = (36 + 2 \times 1) \times 1{,}5 = 57\ mils$$

The second method is based on a table presented in the IPC-2222 standard, Table 9-3, p. 20, in which the diameter of the hole is chosen according to the diameter of the lead and the degree of "manufacturability" - producibility level (A – C). This notion is introduced by the IPC standards that define three levels of complexity (table 3.5).

Level A	General Design Complexity - Preferred situation
Level B	Moderate Design Complexity - Standard
Level C	High Design Complexity - To be used in few situations

Table 3.5: Producibility levels according to IPC

These producibility levels depend on the initial design (project) but also on complexity of the fabrication process and of the manufacturing equipment.

This way, the hole diameters are chosen accordingly to Table 3.6:

	Level A		Level B		Level C	
Hole Diameter	**Mils**	**Millimetres**	**Mils**	**Millimetres**	**Mils**	**Millimetres**
Min Diam. = lead max. diameter +	10	0.25	8	0.20	6	0.15
Max. Diam. = lead min. diameter +	28	0.70	28	0.70	24	0.60

Table 3.6: Hole diameter as function of lead (terminal) diameter

By applying this method for the same terminal of 36 mils for which the datasheet specifies a tolerance of the diameter of 10%, the maximum diameter of 39.6 mils and the minimum of 32.4 mils result. If a level of producibility A shall be achieved, then the diameter of the hole must be chosen between 49.6 mils (39.6+10) and 60.4 mils (32.4+28) or, in metric units, between 1.25 mm and 1.5 mm.

The results obtained for the diameters of the holes by applying the two methods, based in particular on IPC standards are preferred in the case of industrial productions, by industrial soldering processes and should not be considered mandatory for example when the PCB project is made for a prototype and/or manual soldering is used.

Dimensioning of the annular ring for Through-Hole components

Once the diameter of the hole has been determined, the diameter of the circular pad must be determined (in this context the term "land" is used). The difference between the pad diameter and the diameter of the hole is the size of the circular pad, which represents the base area for soldering. Too little soldering area leads to poor soldering, the pad can be destroyed by thermal or mechanical shock or it can be lifted from the board.

An exaggeratedly large pad does not necessarily lead to a better solder joint quality and will only increase the solder alloy consumption and increase the amount of heat needed to make the solder joint.

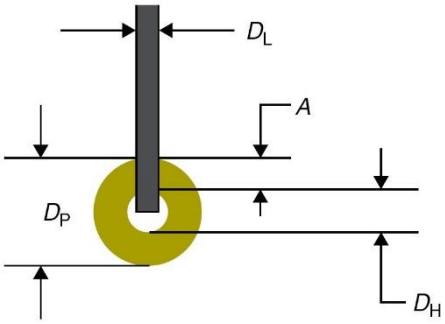


Figure 3.11: Geometry of the annular pad

The IPC 2221 standard is recommended for the calculation of the pad diameter, with the notations in figure 3.11, with the relationship (Mitzner 2009):

$$D_P = a + 2b + c \tag{3.6}$$

with D_P pad diameter, a final hole size ($a = D_H - 2T_P$), b refers to the minimum ring dimensions, having different values for internal and external pad on TOP and / or BOTTOM (1 mil for internal pad, respectively 2 mil for external pad), c is a allowed standard margin that depends on the category of the board according to IPC and has the values 16, 10, 8 mil for the categories Level A, B, respectively C (1mil = 0.0254 mm).

Solder-mask and Solder-paste dimensions

The pads used for Solder-mask layer are typically larger than the pads on the TOP and BOTTOM electrical layers (5 -10 mil). Sometimes, the values with which the pads are increased are required by the PCB manufacturers.

The dimensions for the pads in the Solder Paste layer are chosen by default equal to those of the pads in the outer layers (TOP and BOTTOM). In the PCB Editor program, most footprints in the library do not have defined the Solder Paste layer. The correct choice of pad dimensions is made according to the IPC 7225 standard - Stencil Design Guidelines – a reference for the design of the stencil, the purpose being to ensure an appropriate amount of paste that is transferred to the printed circuit board.

Optimized CERDIP24 PCB footprint design

The main package used by IFRO for the test board design was a ceramic DIP package, having the dimensions presented in figure 3.12.

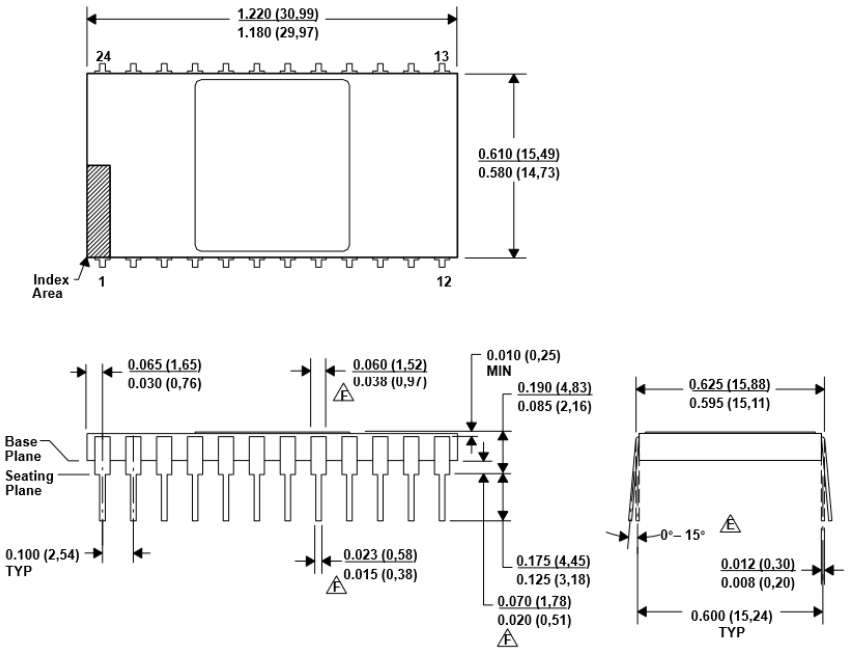


Figure 3.12: CERDIP24 package dimensions

As presented in chapter 2 related to “Pin 1 indicator” for DIP components on electrical layers, where the first pad must be “square” and the rest of pads must be “round”, an optimization activity of UPB was to solve the DFM issue found on the IFRO test board.

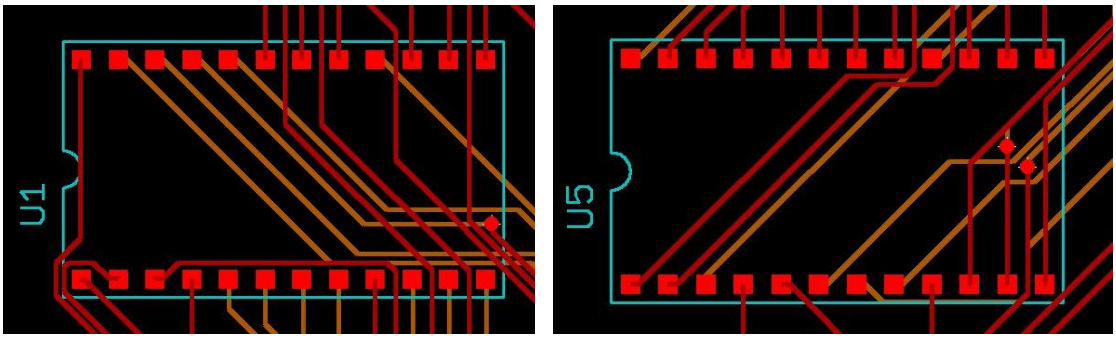


Figure 3.13: U1 and U5 THD DIP footprints presenting the DFM issue of missing "Pin 1 indicator" on electrical layers

In relationship with DFM concepts and principles, the PCB footprint of the CERDIP package (outlines, pads dimensions and drill diameters) must be determined according to mentioned procedure.

IPC offers an automatic calculator of the pad sizes and other footprint items, called the Land Pattern (LP) Calculator. The input data regarding the package must be introduced in the calculator. A screen of the data introduced for the CERDIP package is presented in figure 3.14.

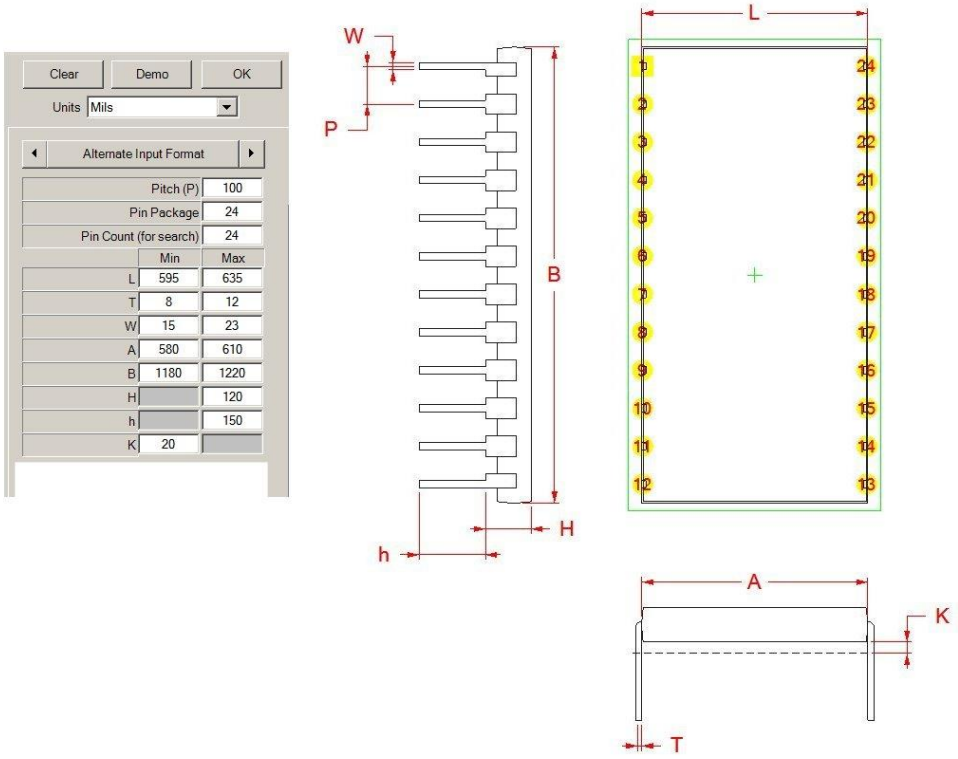


Figure 3.14: LP Calculator screen from IPC with data for CERDIP24 package

Then, in a subsequent window, the LP Calculator displays the results. In this case, the dimension of the pads and the drill diameter are the most important, as can be observed in figure 3.15.

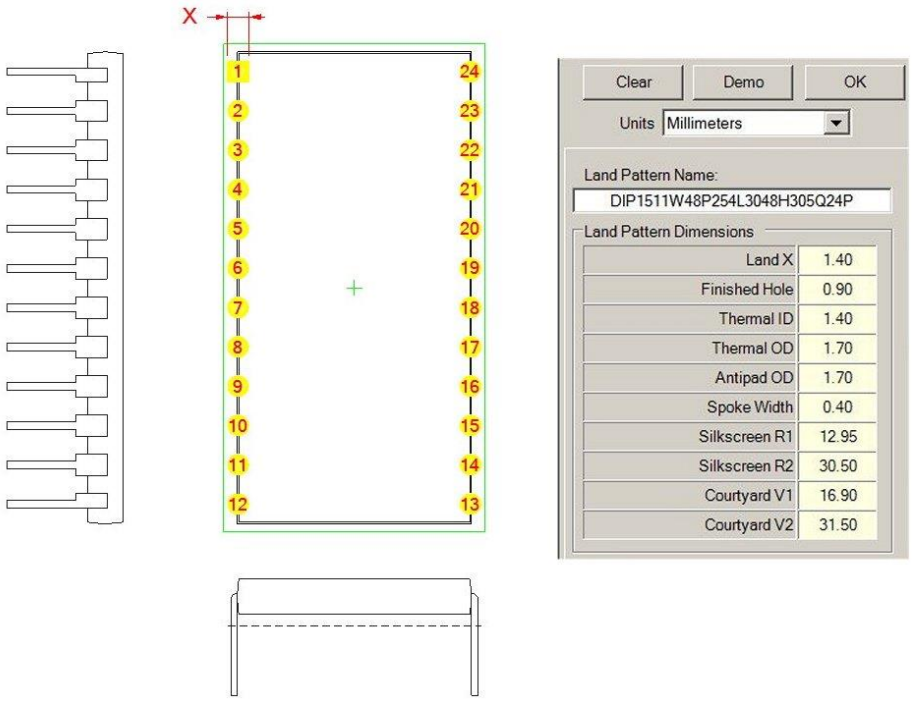
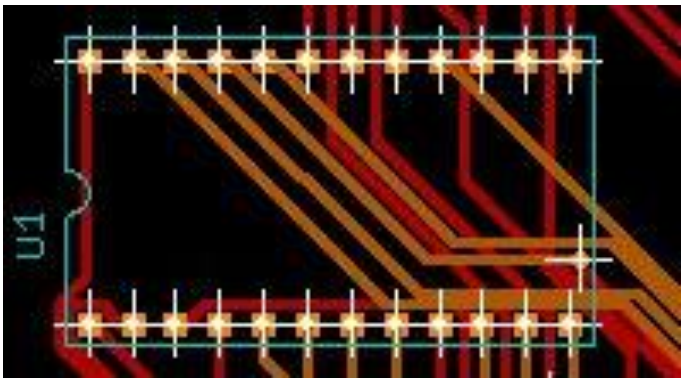
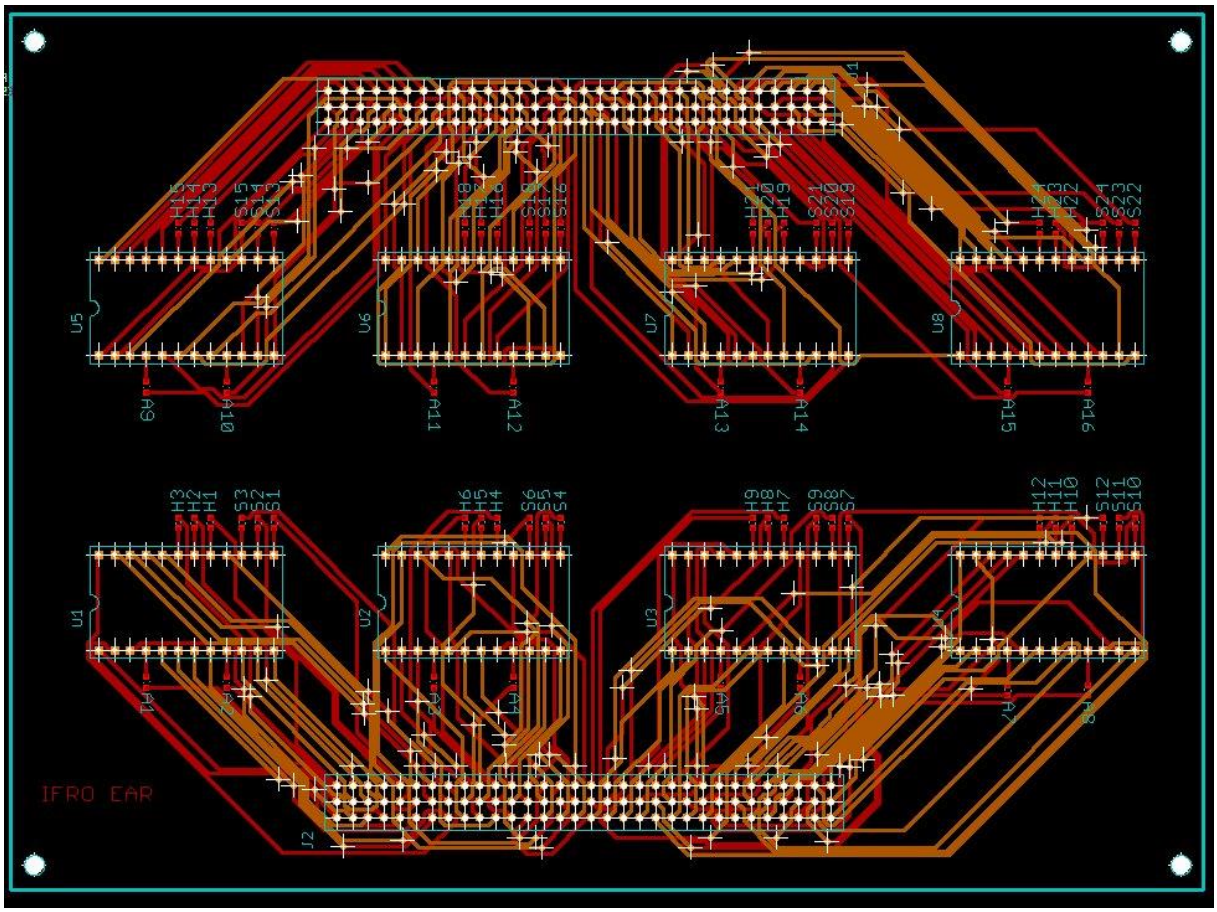


Figure 3.15: Screen of the LP Calculator showing the calculated elements of the footprint for CERDIP24 package

Finally, UPB has checked the correct overlapping between the pads and the drills on the IFRO test board and found that all the drills created during the virtual prototyping stage are totally aligned with the THT and SMT pads of the PCB. Figure 3.16 a) presents a zoom of the U5 DIP package and figure 3.16 b) an overview of the whole test board at the end of the printed circuit board design process, after the mentioned final checking.



a)



b)

Figure 3.16: Checking the overlapping between the pads and the drills on the IFRO test board

4 Conclusions

The Design For Manufacturing (DFM) concept is a concurrent engineering set of techniques developed to bring the down-stream life-cycle product concerns to the forefront of the design process. The DFM process optimizes the future product early in the concept & design phase, in order to ensure that the product will be manufactured in the correct way. In this process, the design of product is optimized as much as possible, being modified to fit the capabilities of the manufacturing facilities. The optimization is done by applying DFM principles, using standard components, eliminating unnecessary devices, integrating multiple components, selecting easy to assemble components and parts, etc. These procedures will not only create a product easy to be manufactured, but also one that uses less material, is of a better quality and involves lower costs, giving to companies a competitive advantage in today's world market.

DFM can be applied in several points in the design and development process (as in the concept generation, schematic capture, layout design and prototype stages). With all the benefits that accompany successful DFM processes, enterprises should apply DFM to any product which will ultimately end up in manufacturing. DFM must be implemented in an environment which is focused and opened to DFM principles, which must be properly balanced with the overall product design objectives and goals. The reason is that some principles can adversely affect the overall product performance, while increasing the manufacturability of the product.

In today's competitive manufacturing environment, DFM has proven to be a successful “tool” in the design and development process. When DFM is successfully implemented, the results can be a better quality, higher productivity, reduced time to market, reduced material usage and considerable cost saving. However, a successful implementation of DFM is not a trivial process. It requires dedication, commitment, and radical organizational changes. Even though many companies apply some forms of DFM, there is a huge difference between those that have successful DFM processes and those that do not have. Because there are several reasons for failure or ineffective DFM, the manufacturing can be really optimized if a series of DFM fundamental concepts and principles are implemented:

- Clear design goals;
- Management's commitment and involvement for change;
- Commitment to concurrent engineering;
- Use of cross-functional teams;
- Team working and communication between persons and teams;
- Designers with better understanding of manufacturing operations;
- Manufacturing engineers involved throughout the entire process;
- Erasing the design-manufacturing barriers;
- Designing for zero defects.

To summarize, Design for Manufacturing is a concept of designing electronic products in order to optimize each phase/factor that leads to their production (fabrication, supplying, assembling, testing, delivering, troubleshooting, etc.) (Plotog and Vărzaru (n.d.)). This concept must ensure the best cost, quality, reliability, be in line with all standards, provide safety in use, have the shortest time to market, and satisfy the customer requirements. All these lead to an improvement in process performance, an increase in profit and an increase in the competitiveness of companies by overcoming manufacturing problems from the early design stage.

5 List of Abbreviations

Abbreviation	Meaning
BGA	Ball Grid Array
BOM	Bill Of Materials
CAD	Computer-Aided Design
CAE	Computer-Aided-Engineering
CAM	Computer-Aided Manufacturing
CERDIP	Ceramic Dual-In-line Package
COB	Chip On Board
DFA	Design For Assembling
DFE	Design For Environment
DFF	Design For Fabrication
DFM	Design for Manufacturing/Manufacturability
DFP	Design For Procurement
DFT	Design For Testing
DIP	Dual-In-line Package
DOE	Design Of Experiments
DRC	Design Rules Check
ERC	Electrical Rules Check
FPT	Fine Pitch Technology
IC	Integrated Circuit
IPC	Association Connecting Electronics Industries (former Institute for Printed Circuits)
IT	Information Technology
JEDEC	Joint Electron Device Engineering Council
LCC	Leadless Chip Carrier

LED	Light Emitting Diode
MELF	Metal Electrode Leadless Face
PCB	Printed Circuit Board
PLCC	Plastic Leadless Chip Carrier
PTH	Plated Through-Hole
PWB	Printed Wiring Board
RoHS	Restriction of Hazardous Substances
SCP	Single Chip Package
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
SO	Small Outline
SOG	Small Outline Gull wing lead
SOIC	Small Outline Integrated Circuit
SOJ	Small Outline J lead
TAB	Tape Automated Bonding
THD	Through-Hole Device
THT	Through-Hole Technology
TR	Thermal Relief
UFPT	Ultra-Fine Pitch Technology

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